3090 PROCESSOR COMPLEX

Functional Characteristics

IBM

Functional Characteristics

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Second Edition (December 1985)

This major revision obsoletes SA22-7121-0. This edition adds information about the vector facility, expanded storage, and machine assists. Changes or additions to illustrations and text are indicated by a vertical line to the left edge of the changed page.

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Preface

This manual is intended for management, programming, and operations personnel; it describes the components and functions of the IBM 3090 Processor Complex Models 200 and 400.

Readers of this manual should be familiar with IBM System/370 (S/370) and IBM System/370 Extended Architecture (370-XA) as defined in the *IBM System/370 Principles of Operation*, GA22-7000, and the *IBM System/370 Extended Architecture Principles of Operation*, SA22-7085.

This manual contains seven chapters, one appendix, a glossary, and a bibliography:

- "Chapter 1. Introduction" summarizes the configurations, design highlights, and programming support of the IBM 3090 Processor Complex.
- "Chapter 2. 3090 Structure" describes the characteristics of the IBM 3090 Processor Complex.
- "Chapter 3. 3090 Processor Unit" describes the the processor unit.
- "Chapter 4. Consoles" describes the interactive consoles in the 3090 Processor Complex and, in particular, the facilities provided by the system console.
- "Chapter 5. 3092 Processor Controller" describes the processor controller.
- "Chapter 6. Error Handling" describes error recovery procedures that are performed automatically by the processor controller, the customer problem analysis procedures, and the remote support facility procedures.
- "Chapter 7. 3090 Feature Descriptions" describes the standard and optional features provided by the 3090 Processor Complex.
- "Appendix A. 3090 Deviations" contains exceptions to the *IBM System/370 Principles of Operation* and the *IBM System/370 Extended Architecture Principles of Operation.*
- "Glossary of Terms and Abbreviations" defines the technical terms and abbreviations used in this manual.
- "Bibliography" lists the manuals that are recommended for use with this manual.

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Chapter 1. Introduction

The IBM 3090 Processor Complex Model 200 (Figure 1-1) and Model 400 are general-purpose data processing systems that provide reliability, performance, and ease of use for commercial, engineering, and scientific applications.

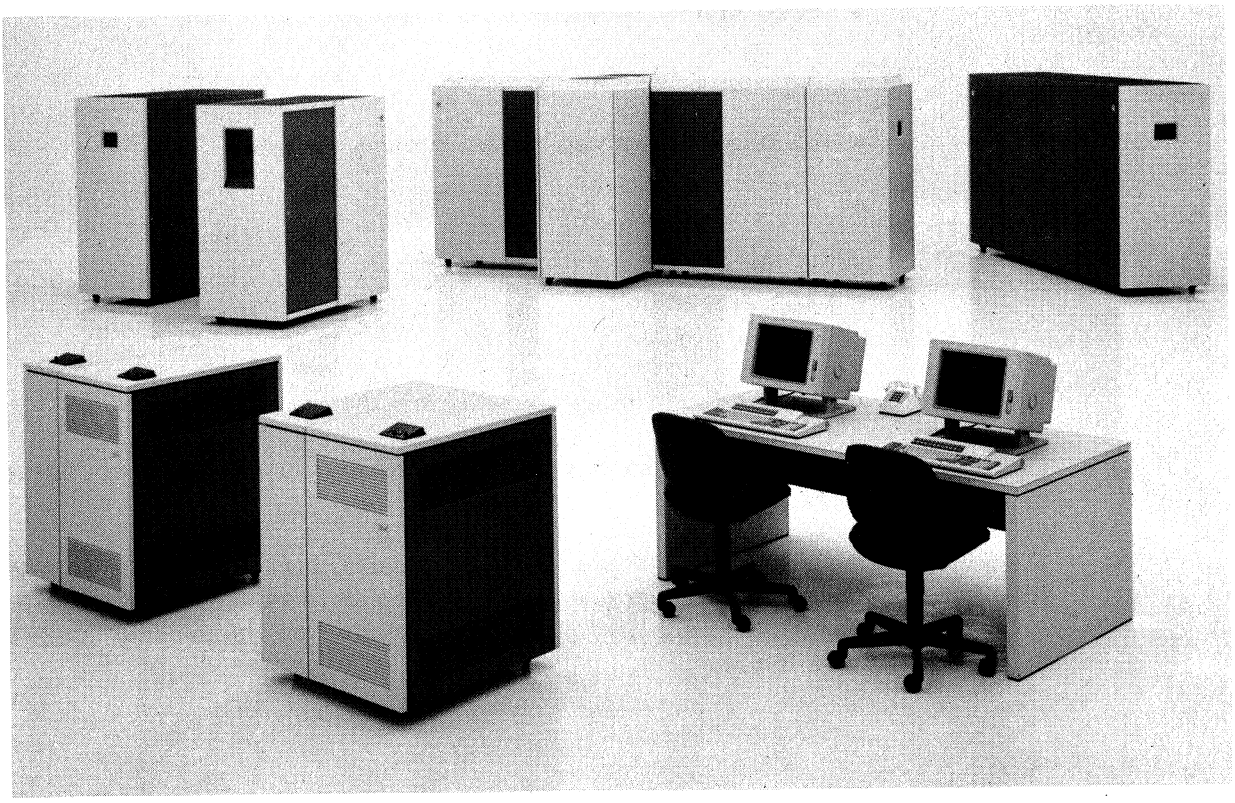


Figure 1-1. IBM 3090 Processor Complex Model 200 (Design Models)

The 3090 is a compatible growth system for the IBM 308x Processor Units. The 3090 Model 200 can be upgraded in the field to a 3090 Model 400.

Summary of 3090 Model 200 and 3090 Model 400 Configurations

The 3090 Model 200 provides the following configuration:

- Two integrated central processors
- A vector facility for each central processor (optional)
- 64M bytes of shared central storage
- Expanded storage (optional):

  64M bytes

  128M bytes

- As many as 48 integrated channels (32 are standard)

The 3090 Model 200 is a two-way (dyadic) processor because the processor complex contains two integrated central processors, each having access to a common central storage, expanded storage, and channels.

The 3090 Model 400 provides the following configuration:

- Four integrated central processors
- A vector facility for each central processor (optional)
- 128M bytes of shared central storage
- Expanded storage (optional):

  128M bytes

  256M bytes
- As many as 96 integrated channels (64 are standard)
- Capability to be partitioned into two dyadic processors similar to two Model 200s

The 3090 Model 400 is a four-way processor because the processor complex contains four integrated central processors, each having access to a common central storage, expanded storage, and channels for single-image operation.

Design Highlights

The 3090 provides high performance and flexibility of use with improved design and technology.

The design of the 3090 incorporates:

- High-level performance
- Optional expanded storage
- Improved technology
- Improved reliability, availability, and serviceability
- Two architectural modes of operation
- Engineering and scientific capabilities

High-Level Performance

High-level performance is achieved by:

- An 18.5-nanosecond (ns) machine cycle time
- A high-speed 64K-byte buffer in each central processor
- Buffer-to-buffer data paths
- The use of emitter-coupled logic (ECL) in the thermal conduction modules (TCMs)
- Optional expanded storage to extend central storage capacity, to reduce paging, and to improve response time
- Optional vector facility on each central processor for improved engineering and scientific performance

Optional Expanded Storage

Optional high-speed, high-capacity expanded storage is available as an integrated part of the 3090 Processor Complex. Expanded storage is available in 64M-byte increments to a maximum of 128M bytes for the Model 200, and 128M-byte increments to a maximum of 256M bytes for the Model 400. Expanded storage improves system response and system performance balancing.

Improved Technology

The 3090 uses large-scale integration that permits as many as 100 high-density silicon chips to be mounted on a multilayered ceramic substrate in a helium-filled module called a thermal conduction module (TCM). TCMs plug into a supporting multilayered circuit board. The use of TCMs and the boards significantly reduces requirements for power, space, cabling, and cooling, while enhancing reliability. Performance is improved because the TCMs use a faster-circuit family of emitter-coupled logic (ECL) instead of transistor-to-transistor logic.

Improved Reliability, Availability, and Serviceability

The 3090 offers improved reliability, availability, and serviceability (RAS) by providing:

- Additional online error detection and fault isolation techniques
- Deferred maintenance capability
- Enhanced remote support strategy

RAS improvements are implemented by the processor controller, which contains two integrated processor elements. The dual processor elements

provide backup for critical processor controller functions and improve 3090 availability.

Two Architectural Modes of Operation

The 3090 can operate in either S/370 mode or 370-XA mode. The mode is selected when the 3090 is initialized. In S/370 mode, the 3090 has full compatibility with System/370. In 370-XA mode, the 3090 has the advantages of System/370 extended architecture and has problem-program compatibility with System/360, System/370, and 4300 processors.

Note: A 3090 Model 400 in single-image operation operates only in 370-XA mode. A 3090 Model 400 in partitioned operation is similar to two 3090 Model 200s, and each side can operate in either S/370 or 370-XA mode.

S/370 mode provides:

- System/370 extended facility
- 3033 extension
- Extended addressing
- As many as 16 channels for Multiple Virtual Storage/System Product (MVS/SP) per channel set or as many as 32 channels for Virtual Machine/System Product-High Performance Option (VM/SP-HPO) per channel set

370-XA mode provides:

- 31-bit addressing that provides a capability of a virtual address range of 2G bytes (2 147 483 648 bytes)
- Bimodal addressing that allows programs written with S/370 mode 24-bit addressing to execute and coexist with programs written with 370-XA mode 31-bit addressing
- Channel path selection and I/O-busy-condition management as hardware functions (rather than system-control-program functions) that provide:
  - As many as four channel paths available to each I/O device
  - Increased I/O device accessibility by allowing each central processor to initiate operations with any of the I/O devices and to handle any I/O interruption conditions
- Support for the Start Interpretive Execution (SIE) instruction by allowing support of guest S/370 or 370-XA virtual machines

Engineering and Scientific Capabilities

Improved engineering and scientific computational performance in a general-purpose architecture are implemented by:

- Rapid floating-point arithmetic
- Very large storage
- High performance channels
- Improved availability
- A powerful instruction set
- Optional vector facility

| *Vector Facility*

The vector facility is optional for each of the central processors of the 3090 Processor Complex Models 200 and 400. Central processors with the optional vector facility provide significantly increased levels of performance for many compute-intensive engineering and scientific applications.

Programming Compatibility

Any program (including its programming support) written for S/370 mode or 370-XA mode operates on a 3090 Processor Complex Model 200 operating in that mode, provided that the program:

1. Is not time dependent.
2. Does not depend on the presence of system facilities (such as storage capacity, I/O equipment, or optional features) when the facilities are not included in the configuration.
3. Does not depend on the absence of system facilities when the facilities are included in the configuration.
4. Does not depend on results or functions that are defined in the appropriate Principles of Operation manual as being unpredictable or model dependent.
5. Does not depend on results or functions that are defined in this manual as being deviations from the appropriate Principles of Operation manual.
6. Does not depend (for 370-XA mode) on the contents of instruction parameter fields B and C on interception of the SIE instruction. See *IBM System/370 Extended Architecture Interpretive Execution,* SA22-7095, for additional information.

7. Does not depend (for S/370 mode) on the presence of the 2K-byte page size, or the presence of storage protection keys associated with 2K-byte blocks of storage.

Any problem state program written for S/370 operates in 370-XA mode, and any problem state program written for S/360 operates in 370-XA mode or S/370 mode, provided that the program:

1. Observes the limitations in the preceding statements.

2. Does not depend on any programming support facilities that are not provided or that have been modified.

3. Takes into account other changes made that affect compatibility between modes. These changes are described in the *IBM System/370 Extended Architecture Principles of Operation,* SA22-7085, and in the *IBM System/370 Principles of Operation,* GA22-7000.

The limitations described in the preceding topic for the 3090 Processor Complex Model 200 also apply to the 3090 Processor Complex Model 400 in single-image operation, and, independently, to each side of a 3090 Processor Complex Model 400 in partitioned operation.

Programming Support

System control programming support (native programming support) is dependent on the mode in which the 3090 Processor Complex is operating. For example, a 3090 operating in 370-XA mode requires a system control program for 370-XA mode.

System control programming support for the 3090 Processor Complex includes:

- S/370 control programs
  - MVS/SP Version 1 Release 3.5

    Note: Expanded storage is not supported. The maximum number of channels per channel set is 16.

  - VM/SP High Performance Option Release 3.6
  - VM/SP High Performance Option Release 4.2
- 370-XA control programs
  - MVS/SP Version 2 Release 1.3
  - VM/XA Systems Facility

Guest Control Programs

Start interpretive execution (SIE) support is provided by VM/XA Systems Facility for the following guest environments:

- MVS/SP Version 1 Release 1 with Release 1 Enhancement
- MVS/SP Version 1 Release 3
- MVS/SP Version 2 Release 1
- VM/SP Release 2.1
- VM/SP High Performance Option Release 3
- VM/SP Migration Aid Release 1 (V=V only)
- VM/XA Systems Facility (V=V only)
- OS/VS1 Release 7 with Basic Programming Extensions Release 3
- VSE/Advanced Function Release 3

Chapter 2. 3090 Structure

The following 3090 characteristics are significant to the processor complex structure:

- Processor complex configuration
- Console and display configuration
- Power and cooling
- I/O operations
- Storage operations
- Data representation
- System security
- Technology
- Processor controller
- RAS considerations

Processor Complex Configuration

The 3090 Processor Complex machines and features are categorized as follows:

- Standard machine requirements of the 3090 Processor Complex.
- Corequisite machine requirements for the operation and maintenance of the processor complex that are ordered separately.
- Optional features for expanding the size, function, or performance of the system that are ordered separately and that are added to the processor complex at the customer's request.

Standard Machine Requirements

Standard machine requirements for the 3090 Processor Complex are:

- One IBM 3090 Processor Complex Model 200 (Figure 2-1) or Model 400
- One IBM 3092 Processor Controller Model 1 or 2
- One IBM 3097 Power and Coolant Distribution Unit Model 1 (two 3097s are required for the 3090 Model 400)

- Two IBM 3180 Display Stations Model 140 (three 3180s are required for the 3090 Model 400)

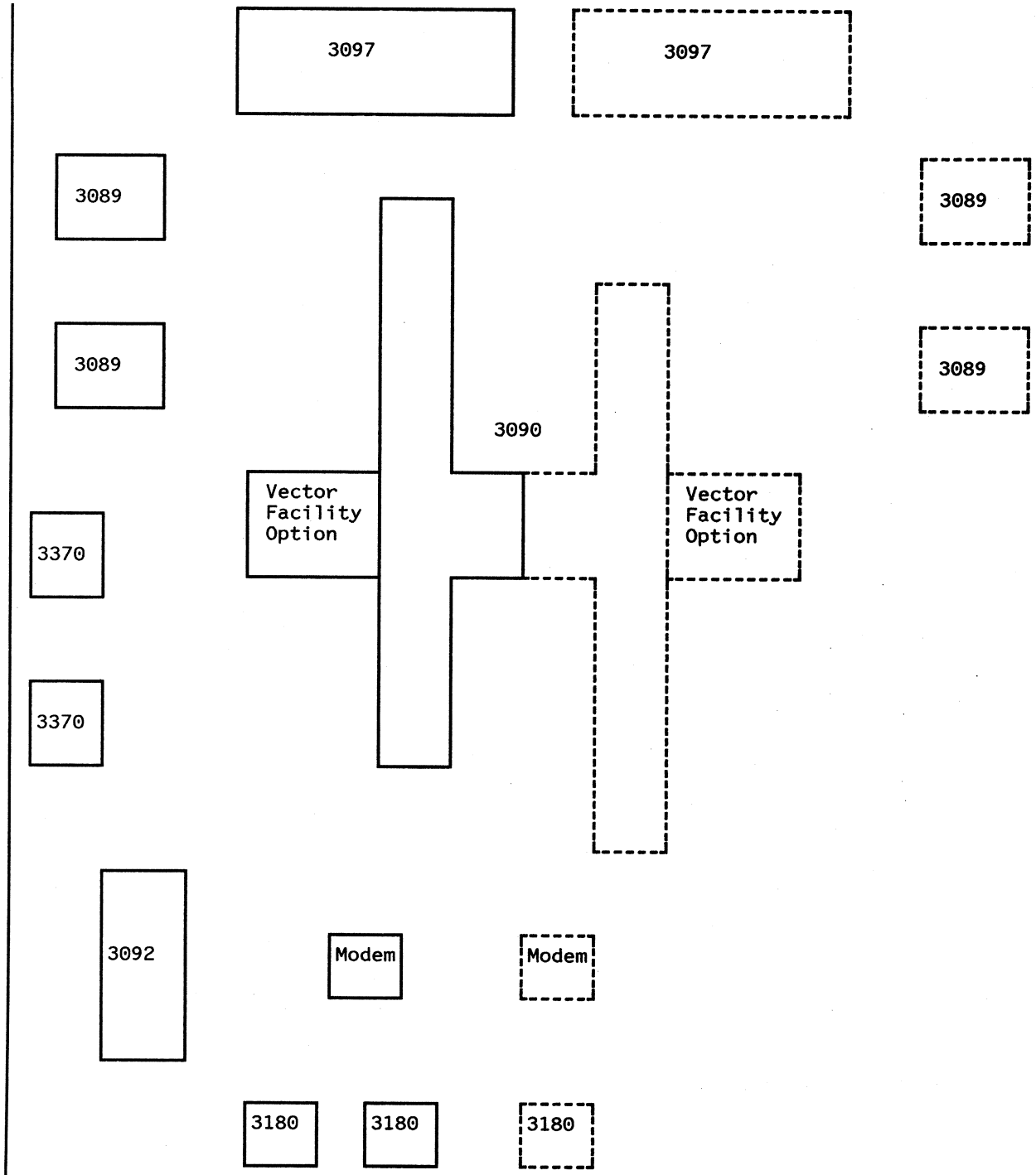


Figure 2-1. IBM 3090 Processor Complex Plan View

Corequisite Machine Requirements

The corequisite machine requirements for the 3090 Processor Complex are:

- Two IBM 3370 Direct Access Storage Model A2 units, each with a string-switch feature.
- Access to a channel-attached IBM 3803 Tape Control Unit Model 2 (or equivalent) and its associated IBM 3420 Magnetic Tape Unit Model 4, 6, or 8 (and compatible 6250 bit-per-inch tape drive), or equivalent. The 3090 Model 400 requires access to two channel paths.
- One (Model 200) or two (Model 400) IBM 3864 Modems Model 2 with an automatic calling unit feature (or equivalent).
- Two (Model 200) or four (Model 400) IBM 3089 Power Units Model 3 (or other 400-Hz power source).
- One (two for a Model 400 operating in partitioned operation) operator display station for system control program (SCP) communication.

Optional Machines and Features

Optional machines and features that may be included are:

- Expanded storage from 64M bytes (Model 200) to a maximum of 256M bytes (Model 400)
- Vector facility for each central processor
- As many as 16 additional channels (for a maximum of 48 for a Model 200) or 32 additional channels (for a maximum of 96 for a Model 400)
- One (two for the Model 400) IBM 3287 Printer Model 1 or 2
- Three (Model 200) or two (Model 400) IBM 3180 Display Stations Model 140

Console and Display Configuration

Physical displays that are required for 3090 operation include:

- One (Model 200) or two (Model 400) displays for system consoles
- One display for a service console
- One (Model 200) or two (Model 400 operating in partitioned operation) displays for operator consoles

The system and service displays are controlled by the processor controller and the operator display is channel attached to the 3090 Processor Complex.

Standard display requirements are two (Model 200) or three (Model 400) 3180 Display Stations Model 140 to be used as system and service consoles.

Corequisite display requirements include one 3180 Display Station or one IBM 3278 Display Station or one IBM 3279 Color Display Station (or equivalent) to be used as operator consoles.

Optional displays include as many as three additional 3180-140s for the Model 200 and as many as two additional 3180-140s for the Model 400. These optional displays are used for one of the following multiple console functions:

- System console
- Service console
- Programming support console
- System console monitor
- Service console monitor

Power and Cooling

Power and cooling are combined in one unit, the 3097 Power and Coolant Distribution Unit (PCDU) Model 1.

Power

The 3097 PCDU provides the 50-Hz or 60-Hz power source for the processor complex and access to the 3089 Power Unit Model 3 or other 400-Hz power source.

The 3097 PCDU contains I/O power sequence control to power on and off as many as 64 control units. With the optional feature for additional I/O power sequence control, as many as 128 control units can be powered on and off.

The Model 400 (with two 3097 PCDUs) provides I/O power sequence control for 128, 192, or 256 control units.

Cooling

The cooling system consists of a closed-loop, distilled water circulating system. Most of the heat generated in the electronic and regulator frames is removed by this cooling system. The coolant is circulated throughout the frames and is returned to the 3097 PCDU for cooling in a heat exchanger, where external connections to customer-supplied chilled water absorb the heat from the cooling system water loop.

The 3097 PCDU maintains controlled temperature and flow rates to the densely packed circuits in the 3090 Processor Complex. The 3097 PCDU contains both the necessary controls to maintain the correct temperature within the self-contained closed loop and an automatic valve to adjust the flow rate of the chilled water.

If a cooling problem occurs because of a malfunction in the operating pump, an alternate pump is switched automatically into the coolant circuit for continued operation.

Input/Output Operations

The following information describes the 3090 Model 200 I/O operations. For a Model 400 in single-image operation (A-side and B-side), the number of channels and central processors is doubled.

I/O operations are handled by the channel subsystem in the processor complex. The channel subsystem provides as many as 48 channels: 32 are standard, 16 are optional. All channels can be configured for block-multiplexer operation and as many as four channels can be configured for byte-multiplexer operation. Any channel not needed for byte-multiplexer operation can be configured for block-multiplexer operation.

Failing channels can be removed from the operating configuration. As many as eight control units can be physically attached to a channel, and each channel can address as many as 256 I/O devices. However, the total number of devices attached, for either Model 200 or 400, is 4096 minus the number of channels defined by using the I/O Configuration Program (IOCP). The way in which the channel subsystem performs I/O operations differs depending on the mode of operation (S/370 or 370-XA mode).

S/370 Mode

In S/370 mode, any channel may be assigned any valid channel address without concern for priority. Logically, channels are organized into two sets (one set for each central processor) with as many as 16 channels allowed in one set for MVS/SP operation and as many as 32 channels allowed in one set for VM/SP-HPO operation. Channel-set switching is a standard feature. If one central processor fails, its channel set can be reassigned (under program control) to the other central processor. The other central processor can then use the two channel sets alternately to continue data processing (with some performance degradation).

370-XA Mode

In 370-XA mode, as many as four channel paths are available to any attached I/O device. During any I/O operation, one of the available channel paths to any specific I/O device is selected. Channel path selection is a hardware function rather than a system-control-program function.

At the start of an I/O operation, a central processor signals the channel subsystem (instead of a single channel, as in S/370 mode) that an I/O operation to a given I/O device is needed. An I/O request is posted to a queue; meanwhile, instruction execution in the central processor continues. Channel path management and the queuing of I/O requests eliminate all busy-condition I/O interruptions encountered in S/370-mode operations.

Channel-to-Channel Connection

Channel-to-channel connection between multiple 3090 Processor Complexes is accomplished by using the IBM 3088 Multisystem Channel Communication Unit (MCCU) Model 1 or 2. Channel-to-channel connection between 3090 Processor Complexes and other IBM processors can be accomplished by using the channel-to-channel adapter (CTCA) feature on those processors that offer it or by using the 3088 MCCU. Both data-streaming and interlock modes are standard. Data-streaming mode provides data transfer as many as 3.0 megabytes per second, independent of cable length. Cable distances of 122 meters (400 feet) between processors and 3088 MCCUs are supported in both data-streaming and interlock modes. The 3088 MCCU Model 1 can interconnect as many as four processor channels and can provide the equivalent function of as many as 126 CTCAs. The 3088 MCCU Model 2 can interconnect as many as eight processor channels and can provide the equivalent function of as many as 252 CTCAs.

Storage Operations

A hierarchical storage structure increases performance and contributes to system reliability. Each central processor contains a 64K-byte high-speed buffer (cache) that handles instruction, operand, and data fetches. Central storage provides 64M bytes of storage capacity for the 3090 Processor Complex Model 200 (128M bytes for the 3090 Processor Unit Model 400), which is shared by the central processors. Expanded storage (an optional feature) is available in 64M-byte increments to 128M bytes for the Model 200, and in 128M-byte increments to 256M bytes for the Model 400. Expanded storage is controlled by the system control program and transfers 4K-byte pages to and from central storage. The system control program can use expanded storage to reduce the paging and swapping load to channel-attached paging devices in a storage constrained environment and a heavy paging environment.

In 370-XA mode, storage addressing is extended from 24 bits to 31 bits, which represents an address range of 2G bytes (2 147 483 648 bytes). In addition, 370-XA mode permits the use of either 24-bit or 31-bit addressing, under program control, and permits existing application programs to run with control programs.

In 370-XA mode, an additional channel command word (CCW) format is provided to permit direct addressing of storage of more than 16M bytes for I/O operations. With this format, channel programs may also reside in storage of more than 16M bytes.

Data Representation

The basic addressable data unit is an 8-bit byte that may be used as one character, two decimal digits, or 8 binary bits. The 3090 provides the following data representation features:

- Efficient use of storage and effective I/O rates for decimal data
- Variable-length fields
- Broad and flexible code conversion
- Decimal arithmetic
- Fixed-point and floating-point arithmetic
- 32-bit words, 64-bit doublewords, and 128-bit extended words (for floating-point arithmetic)
- Instructions for functions such as translate, edit, convert, move, and compare

System Security

Data integrity features and a two-level system access control contribute to a high level of system security. Customer planning and management are responsible for the implementation and adequacy of the following controls, and the use of the privileged operator controls such as display and alter storage.

Data Integrity

Data integrity is maintained through:

- Key-controlled storage protection (store and fetch)
- Low-address storage protection
- Storage error checking and correction
- Parity and other internal error checking
- Segment protection (S/370 mode only)
- Page protection (370-XA mode only)
- Block-multiplexer channel command retry
- Remote support authorization
- Clear reset of registers and main storage

System Access Control

System access control protects against inadvertent system damage by restricting commands and the use of display frames only to persons at specified authorization levels. System access control is implemented through a hierarchical structure such that a user will have access to functions at a specified level as well as all levels below the specified level. Access levels can be defined for the system console and the service console.

Also, the 3180 Display Station provides the following:

- A security keylock on the display that allows authorized access and that prevents unauthorized access.
- User authorization for remote access (remote support facility) necessitates the matching of a user-assigned access code, as well as enablement of automatic dialing.

Technology

The 3090 Processor Complex uses several logic-circuit technologies. The central processor logic is implemented by using emitter-coupled logic (ECL) in thermal conduction modules (TCMs). However, central storage and the processor controller function are implemented by a mixture of monolithic technologies.

The TCM is a helium-filled, encapsulated module that is covered by a cold plate through which chilled water circulates to absorb heat. The TCM measures 125 by 134 by 35 millimeters (4.9 by 5.3 by 1.4 inches) and contains as many as 100 silicon chips mounted on a multilayered ceramic substrate that produces a package containing tens of thousands of logic circuits. TCMs plug into a multilayered circuit board that provides TCM powering and TCM-to-TCM connections. Each central processor consists of nine TCMs and the associated circuit board. Therefore, the major element of a processor complex is designed so that no external wiring or cabling is required.

Processor Controller

The 3092 Processor Controller is a stand-alone support unit that includes dual processors: one active and one backup. The backup processor monitors the active processor to provide a high level of availability.

The 3092 continuously monitors the 3090 Processor Complex operation through direct communication with each component in the processor complex.

The 3092 initializes the system, distributes microcode to writable control storage at initialization, monitors voltage levels and coolant temperature, and provides the control unit function for the attached display stations.

The 3092 also provides extensive error recording, recovery, and diagnostic support for the processor complex.

Reliability, Availability, and Serviceability Considerations

Reliability, availability, and serviceability (RAS) are improved in the 3090 by the reduction of downtime and by using standard features.

Reliability:

- TCM/ECL technology that provides a low intrinsic failure rate
- A dual processor controller that incorporates switchover and initialization of the functional side
- Dual 3370 Direct Access Storage Model A2 units that support switchover
- Multiple security provisions for data integrity and system security
- Alternate input for like functions using service language commands, display frames, and function keys
- Multiple consoles for monitoring functional console activity and for backup

Availability:

- Two (Model 200) or four (Model 400) central processors
- Automatic error detection and correction in both central storage and expanded storage
  - Single-bit error correction and double-bit error detection in central storage
  - Single-bit and double-bit error correction and triple-bit error detection in expanded storage
- Storage deallocation in 2M-byte increments under system program control
- The ability to vary channels offline in single channel increments
- Customer problem analysis to effect recovery without a service call

Serviceability:

- The location of many functional elements on power boundaries
- Automatic fault isolation (analysis routines) concurrent with operation

- Automatic remote support capability
- On-site problem isolation
  - Field-replaceable unit (FRU) isolation
  - Trace tables
  - Error logout recording

Chapter 3. 3090 Processor Complex

The 3090 Processor Complex consists of the following logical components (see Figure 3-1 on page 3-2) that execute instructions and commands and that perform storage and channel operations:

- Two (Model 200) or four (Model 400) integrated central processors
- Vector facility for each central processor (optional)
- Shared central storage
- Shared expanded storage (optional):
- Channel subsystem
- One (Model 200) or two (Model 400) system control elements

The 3090 Processor Complex Model 200 provides the following:

- 64M bytes of central storage
- Expanded storage (optional):

  64M bytes

  128M bytes
- 32 (standard), 40, or 48 channels

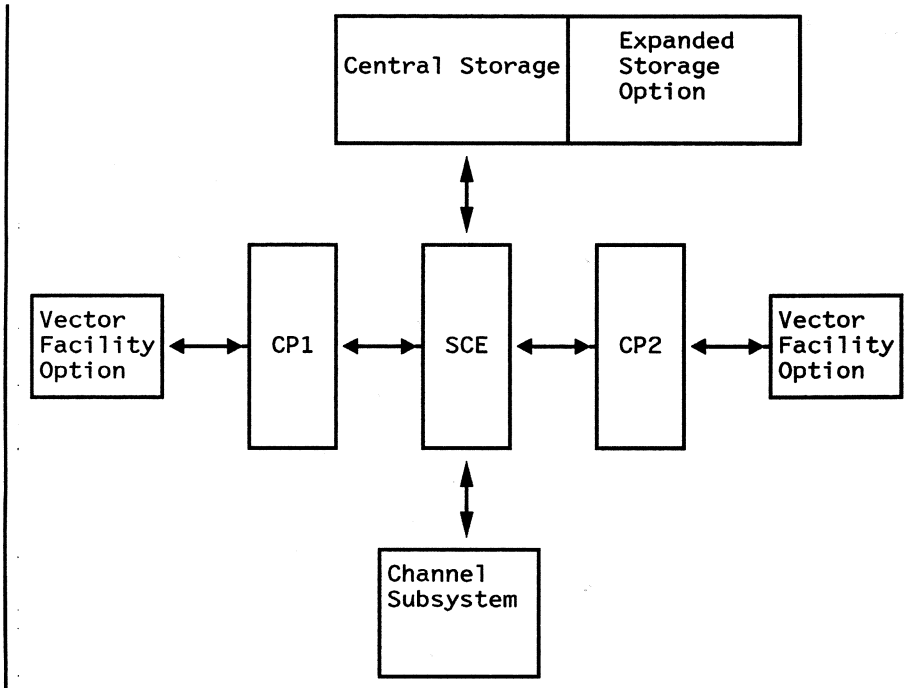
The 3090 Processor Complex Model 400 provides the following:

- 128M bytes of central storage
- Expanded storage (optional):

  128M bytes

  256M bytes
- 64 (standard), 80, or 96 channels

A 3090 Processor Complex Model 200 can be upgraded at a customer's location to a Model 400.



Legend:

CP Central processor
SCE System control element

Figure 3-1. IBM 3090 Processor Complex Model 200 Logical Components

CPU ID

The doubleword whose address is designated by the second operand of the Store CPU ID (STIDP) instruction contains the following information:

- The version code (two hexadecimal digits):
  - 20 (Model 200)
  - 40 (Model 400)
- The central processor (CPU) identification number (six hexadecimal digits):
  - The first digit is the central processor address (as stored by the Store CPU Address [STAP] instruction):

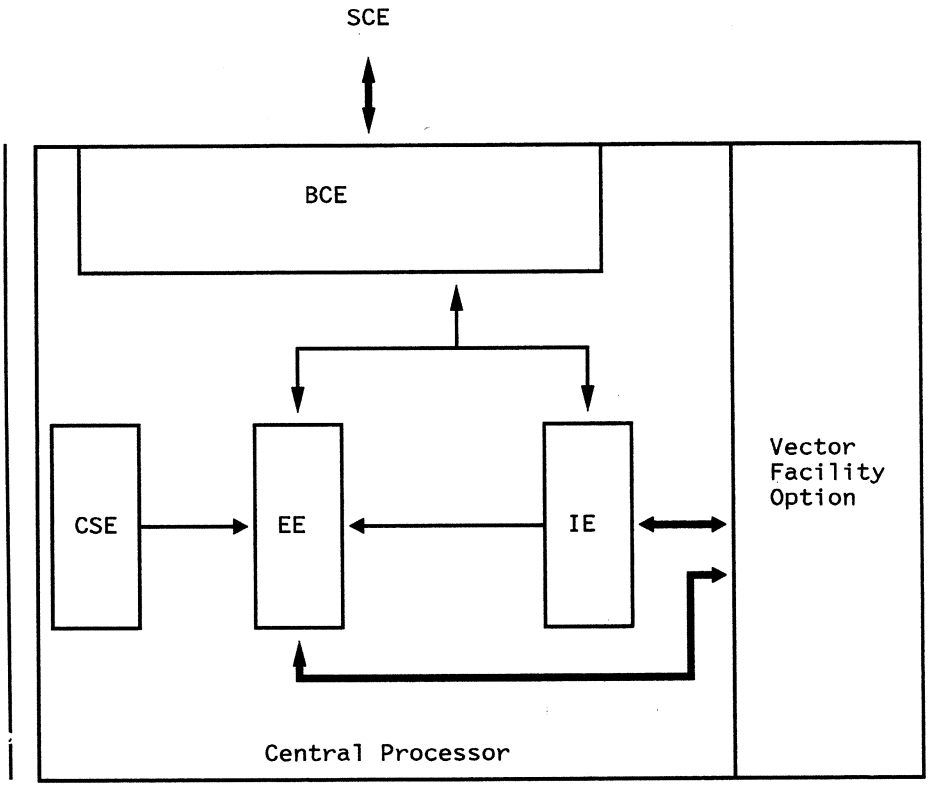
Digit	Model
1 or 2	200
1 or 2	400 (A-side)
3 or 4	400 (B-side)

- The next five digits are selected from the processor unit serial number (both sides of a Model 400 have the same serial number)

- The next four digits are 3090 (for the processor complex number)
- The last four hexadecimal digits are 0000

Central Processors

Each central processor (Figure 3-2) is microcode controlled and contains an instruction element (IE), execution element (EE), control storage element (CSE), and buffer control element (BCE). The CSE fetches microinstructions that control instruction execution in the IE and EE. The BCE controls the transfer of data between central storage and the central processor containing that BCE. Dynamic address translation is an automatic function of the BCE. The central processor machine cycle time is 18.5 ns.



Legend:

BCE Buffer control element
CSE Control storage element
EE Execution element
IE Instruction element
SCE System control element

Figure 3-2. Elements of the Central Processor

Instruction Element

The instruction element (IE) controls the sequencing of all instructions. The IE performs the following operations:

- Decodes instructions
- Calculates addresses
- Sends fetch requests to the BCE (for instructions and data) in central storage
- Determines fetch priority
- Controls storage requests
- Provides the EE with:
  - Operation codes
  - Operands
  - Operand addresses

The IE can process multiple instructions at the same time by handling the instructions in steps. As one instruction is fetched, decoded, and sent to a queue, the IE begins processing another instruction.

Execution Element

The execution element (EE) executes instructions set up by the IE and operates in parallel with the IE. The EE performs the following operations:

- Processes instructions
- Processes interruptions
- Overlaps operations with the IE
- Initiates control functions

The EE performs the logical decisions, arithmetic functions, and many control functions of S/370 and 370-XA architecture instructions. Arithmetic results provided by the EE include the following:

- Fixed point
- Fixed-point multiply
- Convert to binary
- Convert to decimal

- Floating point
- Extended-precision floating point

Control Storage Element

The control storage element (CSE) is the logical element that controls microcode execution in the central processor and contains the supporting control storages and registers that are used by the central processors. The EE is primarily microcode controlled and the CSE contains the microcode that is used for controlling the EE operation.

Buffer Control Element

The buffer control element (BCE) handles all central processor references to and from central storage, performs dynamic address translation, and controls the high-speed buffer.

The BCE includes:

- A 64K-byte high-speed buffer
- A buffer directory
- A translation lookaside buffer (TLB)
- Dynamic address translation (DAT) hardware

The high-speed buffer provides much faster access to instructions than if they were stored in central storage. The high-speed buffer is transparent to programs that are being executed. When data is referred to during instruction execution, the high-speed buffer, the buffer directory, and the TLB are accessed for address comparison.

The buffer directory contains the absolute addresses of central storage for data in the high-speed buffer.

The TLB stores the real address of the referenced page for a translated virtual address in central storage. Therefore, subsequent translations for the same virtual address are not required because the real address is immediately available in the TLB.

Dynamic address translation performs high-speed translation from virtual to real addresses for loading the TLB.

Vector Facility

The vector facility is optional for each central processor of the 3090 Processor Complex Models 200 and 400.

Central processors with the optional vector facility provide significantly increased levels of performance for many compute-intensive engineering and scientific applications. The vector facility is an extension of a central processor's instruction and execution elements. Some of the vector facility characteristics follow:

- The vector facility performs vector arithmetic and logical operations on as many as 128 sets of operands with a single instruction.
- Arithmetic and logical units can produce a 32-bit or 64-bit sum, difference, or product each cycle.
- Compound operations can produce both a product and sum each cycle.
- An instantaneous processing rate for compound operations does 108 million floating-point operations per second (MFLOPS).

System/370 Vector Architecture provides:

- Sixty-three instructions with 171 new operation codes (104 operation codes are for floating point)
- Storage vector addressing
- Contiguous, noncontiguous, and indirect element selection
- Compound multiply-and-add instructions
- Vector results placed in vector registers
- Scalar results placed in scalar registers
- Logical, binary, short floating-point, and long floating-point operands

The vector facility is supported by:

- MVS/XA and VM/SP HPO including automatic support for asymmetric configurations
- VS FORTRAN Extended with auto-vectoring capabilities
- Multitasking facility (MTF) under MVS/XA for assignment of multiple processors to a job
- Engineering scientific subroutine library (ESSL): a set of high-performance mathematical routines compatible with the vector facility architecture of the 3090 Processor Complex

Storage

The 3090 has three levels of storage: a high-speed buffer storage in each central processor, central storage, and optional expanded storage. (The high-speed buffer is described under "Buffer Control Element" in this chapter.) Storage is implemented in monolithic and large-scale-integration technologies.

Central Storage

The Model 200 provides 64M bytes of central storage that is shared by the two central processors. The Model 400 provides 128M bytes of central storage that is shared by the four central processors. A hardware system area (HSA) is reserved within central storage for specific system information and cannot be addressed by user programs. The addressable portion of central storage is synonymous with main storage, as described in the *IBM System/370 Principles of Operation* and the *IBM System/370 Extended Architecture Principles of Operation.*

A central storage controller contains the logic for:

- Data storage and retrieval for the processor complex
- Central storage communication with the processor complex (by means of the system control element)
- Communication with and control of the optional expanded storage
- Error checking and correction (ECC)

Hardware System Area

As part of the initial microprogram load (IML), at least 288K bytes (294 912 bytes) of central storage are selected for use as the hardware system area (HSA). The HSA, which is unavailable for program use, contains:

- Copies of microcode
- A unit control word (UCW) for each configured I/O device
- Message buffers
- Tables
- Directories
- Trace information

The HSA cannot be accessed by conventional (program) storage references.

Depending on the number of UCWs required in the configuration, additional central storage may be required for the HSA. Expansion of the HSA occurs automatically as UCWs are added. HSA expansion for all

purposes can be to 1M byte (1 048 576 bytes) for each partition with the maximum number of devices supported equal to 4096 minus the number of channels defined by the I/O Configuration Program (IOCP).

Error Checking and Correction

Error checking and correction (ECC) code bits are stored with data in central storage. Single-bit errors detected during data transfer are corrected. Multiple-bit errors are flagged for follow-on action.

Data paths from the central processors and the channels are checked for parity. Parity bits are included in each command or data word.

Frame Deallocation

A dynamic page deallocation technique, under system program control, temporarily recovers some double-bit failures and allows the operating system to deallocate the failing page frame if the page is not fixed to that page frame. In these instances, the job is not terminated (abended) and processing continues normally. Central storage may be deallocated in 4K-byte increments under system program control. At the option of the customer, maintenance service may be deferred until a predetermined amount of central storage has been deallocated.

Key-Controlled Storage Protection

Key-controlled storage protection provides both store and fetch protection. It prevents the unauthorized access or modification of information in central storage.

Each 4K-byte block of storage is protected by a 7-bit storage key. For processor-initiated store operations, access key bits 0-3 from the currently active program status word (PSW) are compared with bits 0-3 from the storage key associated with the pertinent 4K bytes of storage to be accessed. If the keys do not match, the central processor is notified of a protection violation, the data is not stored, and a program interruption occurs. The same protection is active for fetch operations if bit 4 of the storage key (the fetch protection bit) is on.

Expanded Storage

Expanded storage is an optional high-speed storage and is available in 64M-byte increments to a maximum of 128M bytes for the Model 200, and in 128M-byte increments to a maximum of 256M bytes for the Model 400. Transfer to and from central storage is in 4K byte pages. Data movement between central storage and expanded storage is controlled by the system control program. No data can be transferred to expanded storage without passing through central storage. Expanded storage reduces the paging and swapping load to channels.

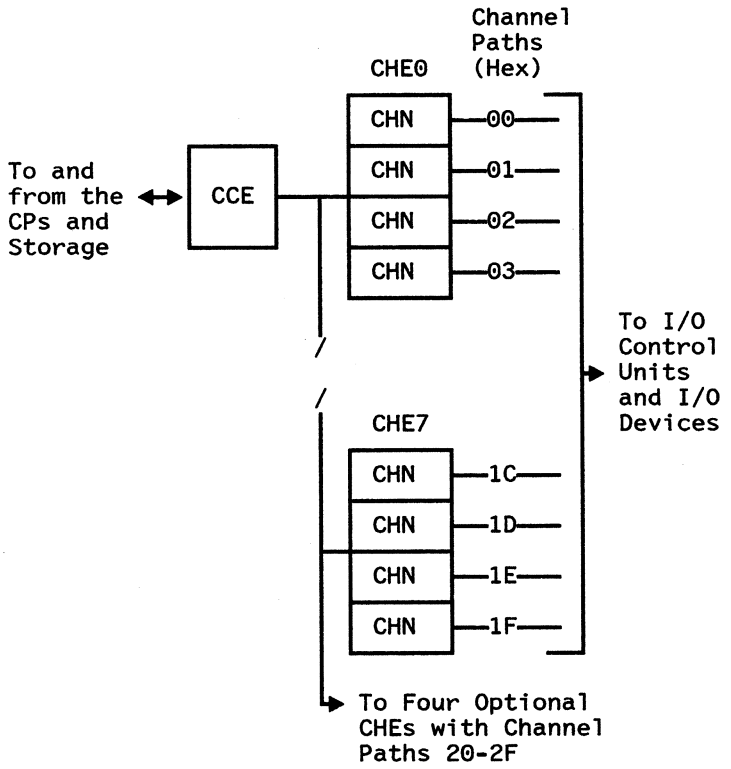
Error Checking and Correction

Error checking and correction (ECC) code bits within expanded storage are used to permit the following:

- Single-bit and double-bit error detection and correction
- Triple-bit error detection
- Some multiple-bit error detection

Unrecoverable errors are flagged.

Channel Subsystem



Legend:

CCE Channel control element
CHE Channel element
CHN Channel server
CP Central processor

Figure 3-3. Channel Subsystem (Example of One Subsystem)

A 3090 Model 200 has one channel subsystem (CSS) and a Model 400 has a CSS on each side (Figure 3-3). In single-image mode, the two CSSs of the Model 400 appear as a one large CSS to the control program.

A CSS consists of one channel control element (CCE) and as many as 48 channels. Each channel interface is controlled by a channel server (CHN), and each group of four CHNs is controlled by a channel element (CHE).

For each CSS, 32 channels are standard and 16 additional channels are optional (in increments of eight). As many as four channels can be configured for byte-multiplex operation; all the others must be configured for block-multiplex operation.

In byte-multiplex operation, channels can be used either in byte-multiplex mode or in burst mode. Byte-multiplex mode permits the concurrent operation of several relatively slow-speed I/O devices.

In block-multiplex operation, channels can operate either in interlocked (high-speed transfer) mode or in data-streaming mode. Data rates can be as high as 3.0 megabytes per second for data-streaming mode. All channels configured for block-multiplex operation may be attached to control units that can operate in high-speed transfer mode or in data-streaming mode.

The CSS handles all I/O operations for the central processors. The CSS controls communication between a configured channel and the control unit and device. The channel, control unit, and device configurations are defined to the channel subsystem by the I/O configuration data set (IOCDS) that is selected at system initialization. The IOCDS is created by the I/O Configuration Program (IOCP) and is stored on the 3370 Direct Access Storage devices that are attached to the processor controller.

At initialization, the IOCDS information is used to build necessary control blocks in the hardware system area (HSA) of central storage.

Channel Control Element

The channel control element (CCE) interacts with central storage, the central processors, and the channels to:

- Initiate and end all channel operations
- Provide central storage access control
- Assign priorities for I/O operations

Channels

The channels control all data flow between the CCE and the control units by using the I/O interface sequences.

System Control Element

The system control element (SCE) accepts and processes storage requests from the central processors and the channel subsystem. The SCE analyzes each request and performs the following actions:

- Establishes request priority
- Performs cross-interrogation (to ensure that the requester receives the most recent copy of data that is shared)
- Processes requests
- Performs error checking
- Performs error reporting
- Handles request responses

Chapter 4. Consoles

The 3090 Processor Complex Model 200 requires two physical displays: one display for a system console and one display for a service console. The system control program requires a third physical display for use as the operator console.

The 3090 Processor Complex Model 400 requires three physical displays: two displays for system consoles and one display for a service console. The system control program requires two additional physical displays for use as operator consoles.

Additionally, the 3092 Processor Controller supports three (Model 200) or two (Model 400) optional physical displays. Each of these physical displays can be used as a:

- System console
- Service console
- Programming support console
- System console monitor
- Service console monitor

Any physical display that is attached to the 3092 can be assigned as multiple logical consoles. A console assignment frame is provided for assigning selected logical consoles to a specified physical display. The Swap Cons function key on the display keyboard is used to rotate the logical consoles assigned to a given display. The 3180 Display Stations Model 140 (Figure 4-1) attach to a 3092.

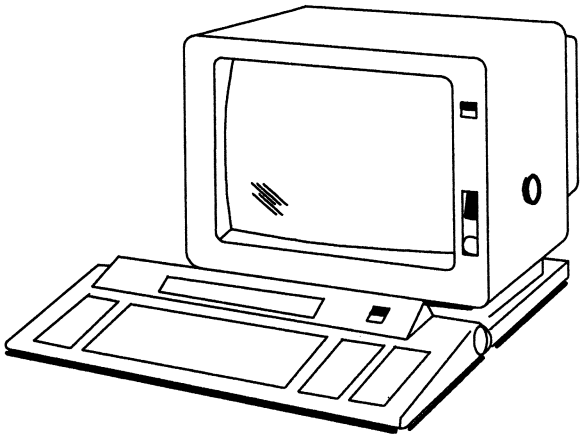


Figure 4-1. IBM 3180 Display Station Model 140

The 3180 has an etched screen that reduces glare and fingerprints. Useful operator information (indicators) is displayed on the bottom line (line 25) of the screen outside the data area. Alternate cursor selection, cursor blink, and normal or reverse character image are also available. The screen can

be tilted, swiveled, raised, or lowered to change the angle for the operator. The slimline keyboard slope can be adjusted for user comfort to 6, 12, or 18 degrees.

System Console Interactive Facilities

The following functions provide additional user control and flexibility in system operation:

- System definition
- System activity display (SAD)
- I/O configuration data set (IOCDS) content
- I/O problem determination (IOPD) information

System Definition

A system definition display frame provides selections to:

- Supply a unique system name that is displayed on line 24 (system status line) of the screen
- Identify the frame that is to be displayed automatically after a power-on reset
- Enter initial program load (IPL) information (device identification and target central processor) for S/370 and 370-XA modes of operation for automatic IPL following a power-on reset

System Activity Display

A maximum of 24 system activity display (SAD) frames can be defined to provide extensive flexibility in the different types of system activity that can be displayed. Frames can be defined to display central processor and channel activity pertinent to certain work shifts or types of jobs. SAD frame definition allows the customer to request that as many as 17 high- or low-usage channels or channel paths be dynamically identified and displayed.

A SAD index lists by number all defined SAD frames with their unique names (if specified when defined).

I/O Configuration Data Set Content

Four I/O configuration data sets (IOCDSs) are available to provide flexibility to change I/O configurations. Two IOCDS display frames can be invoked that provide information about specified control units and devices in the I/O configuration that is defined for the IOCDS currently in effect. The two frames provide the following:

- Information about all control units (CUs) that are associated with a specified channel. The displayed information includes CU machine type, attached channel paths, protocol (data-streaming or interlock), and port addresses.
- Information about all devices that are accessible from a specified channel path.

I/O Problem Determination Information

Two sets (one set for S/370 mode and one set for 370-XA mode) of I/O problem determination (IOPD) frames are available to display I/O status.

Frames for 370-XA mode include status information about all installed channel paths, specified subchannel content, shared control units, and device configuration.

Frames for S/370 mode include status information about all installed channels by channel set, specified device address control block (DACB) content, and I/O transaction area (IOTA) content.

IOPD frames provide the user with extensive I/O information and are helpful in identifying I/O problems.

Chapter 5. 3092 Processor Controller

The 3092 Processor Controller Model 1 (Figure 5-1) or Model 2 monitors and controls the status of all physical units within the 3090 Processor Complex.

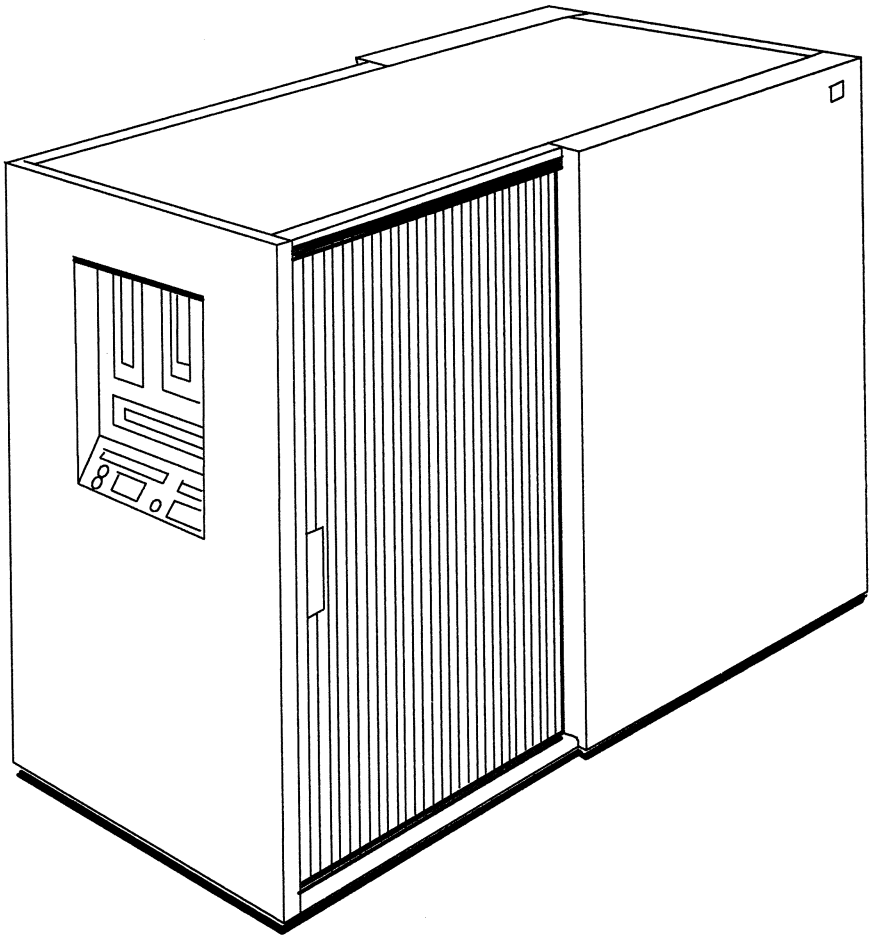


Figure 5-1. IBM 3092 Processor Controller Model 1

The 3092 supports:

- Power on and power off (including I/O units)
- System personalization for S/370 or 370-XA mode of operation
- System initialization
- Control of the configuration of hardware elements
- Control unit function for required and optional consoles and an optional printer
- Monitoring of power supplies, temperature, and coolant flow rate
- Control and assistance for error recovery

- Automatic analysis of data (analysis routines) for field-replaceable unit (FRU) isolation
- Collection and storage of error data (logout data) for later analysis
- Full processor complex remote support capability
- Problem analysis procedures for the customer
- Collection of information for system activity display (SAD) frames
- Collection of information for I/O problem determination (IOPD) frames
- Collection of status information for customer problem analysis (PA) frames

Corequisites

The 3092 requires the following corequisites for full processor complex support:

- Two 3370 Direct Access Storage Model A2 units. (Each 3370 requires a string-switch feature.)
  - One 3370 is active and contains microcode for initialization, operation, and service
  - One 3370 is for backup and is a duplicate of the active 3370
- Access to a channel-attached 3803 Tape Control Unit Model 2 (or equivalent) and its associated 3420 Magnetic Tape Unit Model 4, 6, or 8 (and compatible 6250-bpi tape drive), or equivalent.
  - The tape unit is used to install engineering changes and to reload the 3370s if required
  - Valid addresses for the tape unit are hex 00-9F and B0-FF

  Note: The Model 400 requires access to two channel paths.
- One 3864 Modem Model 2 with an automatic calling unit feature (or equivalent).
  - The modem is required to communicate with the remote support facility (RSF)
  - If the customer does not authorize automatic remote service, manual dial-up can be used

Note: The 3092 Model 2 requires two 3864 Modems Model 2 (or equivalent).

System Power Panel

The 3092 contains the control (System Power) panel (Figure 5-2) that includes switches for power on, power off, and emergency power off and indicators for power status and service mode.

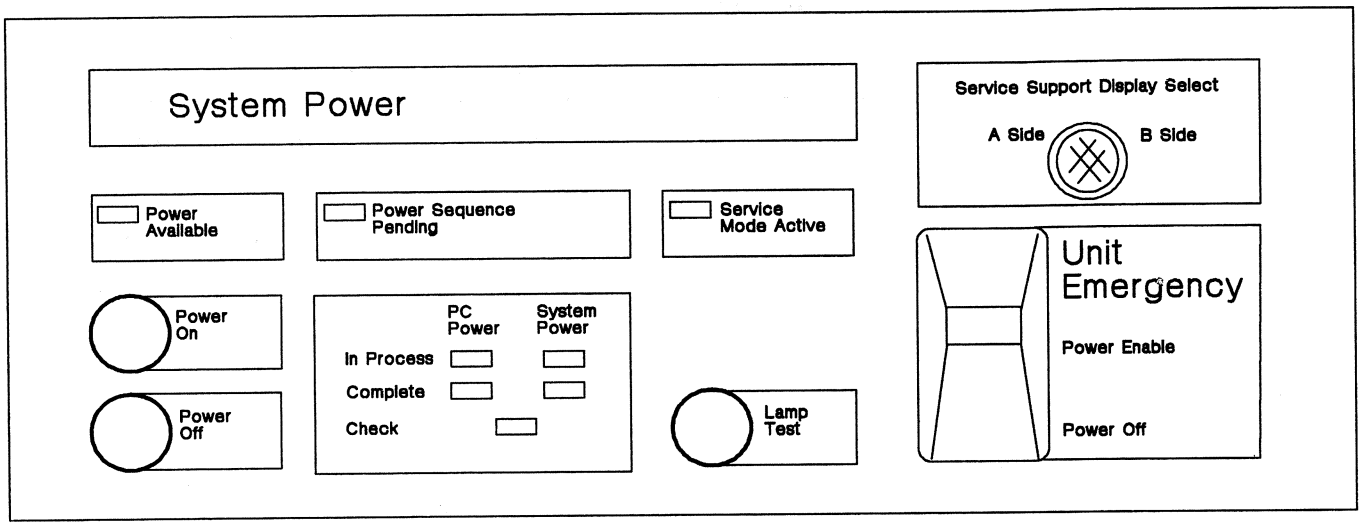


Figure 5-2. System Power Panel

Dual Support Processors

The 3092 contains dual processors (A-side and B-side). One is the active processor and the other is the backup processor. The backup processor monitors the active processor to help maintain availability. In most cases, if the active processor fails, a switchover to the backup processor occurs.

When the Power On pushbutton is pressed, both sides (A-side and B-side) automatically power on and an IML and IPL of both sides occur. The battery-operated clock (BOC) is read and the processor controller time-of-day (TOD) clock is set. Each side communicates its state to the other side to set the active and backup sides. If both sides are functional, the A-side is active, and the B-side is backup. If both sides are functional but the state of the 3370s differs, the side with the most current 3370 is active. If one side is not functional, the functioning side is active.

Note: The 3092 Model 2 uses the same concept for 3090 Model 400 single-image operation. For partitioned operation, the A-side of the 3092 controls the A-side of a partitioned Model 400, and the B-side of the 3092 controls the B-side of a partitioned Model 400.

Operation Monitoring and Control

The 3092 monitors and controls the operations of the 3090 Processor Complex. The 3092 initializes and sequences power to all 3090 components and to all interconnected I/O control units that are under power-sequence control. During initialization of the 3090 Processor Complex, the 3092 validates areas of central storage as error-free data locations, records failing storage locations, and assigns the hardware system area in central storage based on contiguous error-free storage locations. After power sequencing is complete, the processor controller performs an initial microprogram load (IML).

During processing, the 3092 monitors voltage levels and coolant flow rate. If the coolant flow rate decreases or stops, the second pump in the 3097 is switched into the coolant circuit to avoid thermal shutdown.

Error Recovery

The 3092 logs errors as they occur and then analyzes them for service personnel. Failure symptoms, saved at the time of a malfunction, are analyzed on a time-sharing basis with other processor controller functions; this operation is concurrent with operation of the processor complex.

The 3092 saves the symptoms of these errors, correlates multiple symptoms, performs error analysis, and isolates the failure to the failing FRU or group of FRUs. When automatic error-recovery attempts fail or the error occurs frequently, failure information is displayed on the system console, and an audible alarm is sounded to alert the operator of a problem requiring action. During IML, similar notification to the operator occurs when loss of storage exceeds a threshold that may degrade system performance.

Configuration

The 3092 can be used to initiate configuration changes in:

- Central storage
- Central processors
- Online channels

However, operator-initiated action through the system control program is the preferred method of reconfiguration because it makes both hardware and software changes as a single, integrated action.

Remote Support Facility

The remote support facility (RSF) support consists of three parts:

- RSF configuration
- RSF authorization
- RSF call details

RSF Configuration

At installation, the RSF is tailored to the customer's requirements. Two RSF configuration display frames are available for the customer and the service organization to specify remote support facility information. These specifications include:

- As many as four telephone numbers for remote support access
- Type of access equipment available (for example, manual dialing, automatic dialing, automatic calling)
- Agreed-on service update schedule
- Allowance or disallowance of incoming and outgoing calls
- Unique customer access code
- Customer and IBM information
  - Responsible customer personnel
  - Location of the system at the customer's installation
  - Customer's business, system console, and modem telephone numbers
  - IBM branch office number and telephone number
  - Prime shift and off-hour shift dispatcher's telephone numbers

The specified information can be changed at any time by invoking the frames and by entering the revised data.

RSF Authorization

No incoming or outgoing calls are allowed without customer authorization.

Customer authorization includes the following:

- Reason for call
- Type of call: outgoing, incoming, automatic call, manual dialing

- Name of the person at the customer location to be contacted
- Whether a service representative is on-site
- Whether the system is immediately available
- Whether RSF can be enabled, can be deferred, or is not authorized

RSF Call Details

Details of all RSF calls (both incoming and outgoing) are recorded and each call is listed on an RSF log index. The RSF log index can be displayed and any call that is listed can be selected from the index. The RSF log index shows the date, time, status, and reason for the call. When a call is selected, the first of a set of frames is displayed. The frames contain detailed information about the selected call.

See "Chapter 6. Error Handling" for information about customer problem analysis and RSF procedures.

Chapter 6. Error Handling

The 3092 Processor Controller automatically performs certain error recovery procedures. If automatic error recovery is not successful, a set of problem analysis frames and procedures are available to facilitate recovery by the user for certain types of failures, and remote support facility (RSF) procedures are available for all failures.

Automatic Error Recovery

Error handling by the processor controller provides both automatic recovery from many hardware malfunctions and provides reporting by machine- or channel-check interruption.

Error recovery functions are provided for errors in central storage and for channel errors. When an error is detected, the 3092 automatically performs error analysis procedures to isolate the malfunctioning area directly and to identify (if applicable) the field-replaceable unit (FRU) or group of FRUs. These procedures include problem recognition, recording, and diagnosis.

Error Checking and Correction

Error checking and correction in central storage provides automatic single-bit error detection and correction of all data read from central storage. Error checking also detects all double-bit errors and some multiple-bit errors of the data read from central storage, but does not correct the errors.

Some double-bit errors are temporarily recovered to allow the system control program an opportunity to deallocate the failing page frame.

Error checking and correction in expanded storage provides automatic single-bit and double-bit error detection and correction of all data read from expanded storage. Error checking also detects all triple-bit errors and some multiple-bit errors of the data read from expanded storage, but does not correct the errors.

Parity checking is used to verify other data in the processor complex that is not contained in central or expanded storage.

Machine-Check Handling

When a machine check occurs, the 3092 collects the error information and enters it in a log. The central processor then presents a machine-check interruption to the system control program.

All machine-check interruptions store a doubleword that contains a machine-check interruption code. Bits that are not assigned or are not implemented are stored as 0's. Certain bits in control register 14 are

associated with machine-check handling. The 3090 uses bits 3 through 7 in 370-XA mode, and bits 4 through 7 in S/370 mode.

When a malfunction makes it undesirable or impossible to continue processing, the central processor enters the check-stop state. The central processor always enters the check-stop state when the following occurs:

- PSW bit 13 is 0 and an exigent machine-check condition is generated
- Another exigent machine-check condition is detected during the execution of an interruption that was caused by an exigent machine-check condition
- The machine-check interruption code cannot be stored or the new PSW cannot be fetched during the execution of an interruption
- Invalid ECC is detected in the prefix register

The central processor is removed from the check-stop state by a CPU reset.

Note: When multiple central processors are part of the configuration, the processor controller generates a malfunction external interruption to all the configured central processors. If the processor controller cannot identify which central processor should be put into the check-stop state, all central processors are put into the check-stop state.

Figure 6-1 shows the machine-check interruption codes.

Mode			
S/370	370-XA	Bit	Meaning
X	X	0	System damage
X	X	1	Instruction processing damage
X	X	2	System recovery
X	NA	3	Interval timer damage
X	X	4	Timing facility damage
X	X	5	External damage
NA	X	9	Channel report pending
NA	X	11	Channel subsystem damage
X	X	14	Backed up
X	X	16	Storage error uncorrected
X	X	17	Storage error corrected
X	X	18	Storage key error uncorrected
X	X	19	Storage degradation
X	X	20	PSW-EMWP validity
X	X	21	PSW mask and key validity
X	X	22	PSW program mask and condition code validity
X	X	23	PSW instruction address validity
X	X	24	Failing storage address validity
X	X	26	External damage code validity
X	X	27	Floating-point register validity
X	X	28	General register validity
X	X	29	Control register validity
X	X	31	Storage logical validity
X	X	32	Indirect storage error
X	X	34	Delayed access exception
X	X	46	CPU timer validity
X	X	47	Clock comparator validity

Legend:

X Active for this mode of operation
NA Not active for this mode of operation

Figure 6-1. Machine-Check Interruption Codes

I/O Operations

Errors detected by the channel subsystem are reported to the central processors as I/O interruptions or machine-check interruptions. I/O interruptions report the following hardware-related conditions:

- Interface control check (IFCC)
- Channel control check (CCC)
- Channel data check (CDC)

Machine-check interruptions include the following:

- Unrecoverable errors (retry attempts are unsuccessful)
- Persistent errors (retry attempts can be made, but the error threshold is exceeded)
- Serious channel errors that require immediate reporting or cannot be reported as an IFCC or CCC with an I/O interruption

Problem Analysis

To attempt recovery before initiating the remote support facility, the user can invoke problem analysis from the system console index frame. If the problem was caused by a power malfunction, the first of a set of power status problem analysis frames is displayed. If the problem was caused for some other reason, the first of a second set of problem analysis frames is displayed.

Power Malfunction

To assist recovery from a power malfunction, the first set of problem analysis frames displays this information:

- The status of as many as 24 power boundaries
- A list of suggested recovery actions
- Defined service action

Other Malfunctions

Status information is displayed for the central processors, hardware, interface control checks, and channels or channel paths. Based on the status information, the customer can select any of a variety of problem analysis categories that include:

- Non-I/O hardware errors
- Unsuccessful IPL
- Enabled or disabled wait state
- Interface control checks (IFCCs)
- I/O device errors
- Operator console lockout

Each procedure in the problem analysis gives current status information for that type of malfunction, and then lists possible recovery actions. The IOPD frames may also be used when troubleshooting IFCC and I/O device problems. If the attempt at recovery fails and if remote support is required, a selection from the frame invokes the RSF authorization frame.

Remote Support Facility

A priority message is displayed when:

- The processor controller detects a failure that requires service
- The remote support facility requires remote console control (from the remote support center)
- An automatic service update must be done

A customer can also initiate remote support from the problem analysis procedures or by invoking the RSF authorization frame and establishing the remote connection.

After the service request is authorized, a telephone number is automatically dialed over the public switched network to establish a connection with a remote modem. The remote modem acknowledges the connection and the remote support facility is enabled.

When the remote support facility is connected by the data link, the remote support facility has access to the 3090. Control of the 3090 system can be passed to the remote support facility, and the 3090 Processor Complex can be manipulated by remote control.

Chapter 7. 3090 Feature Descriptions

The features described in this chapter are categorized into three groups:

- Features dependent on architectural mode (Figure 7-1 on page 7-2)
- Features that provide programming assists (Figure 7-2 on page 7-4)
- Features not dependent on architectural mode (Figure 7-3 on page 7-5)

The brief descriptions of features in this chapter include an indication of whether the function is a standard or host-program feature of that mode on the 3090. Additional information about the mode-dependent features (Figure 7-1 on page 7-2) can be found in the following manuals:

- *IBM System/370 Principles of Operation*, GA22-7000
- *IBM System/370 Extended Architecture Principles of Operation*, SA22-7085
- *IBM System/370 Extended Architecture Interpretive Execution*, SA22-7095

Feature	S/370 Native	S/370 (SIE) Guest	370-XA Native (Host)	370-XA (SIE) Guest
Basic control (BC) mode	Std	Std	-- (1)	-- (1)
Bimodal addressing	--	--	Std	Std
Branch and save	Std	Std	Std	Std
Byte-oriented operand	Std	Std	Std	Std
Channel indirect data addressing	Std	Host	Std	Std
Channel-set switching	Std	Host	-- (2)	-- (2)
Channel subsystem	--	--	Std	Std
Clear I/O	Std	Host	-- (2)	-- (2)
Command retry	Std	Host	Std	Std
Conditional swapping	Std	Std	Std	Std
CPU timer and clock comparator	Std	Std	Std	Std
Extended-precision divide	--	--	Std	Std
Extended-precision floating point	Std	Std	Std	Std
Extended real addressing (26 bit)	Std	Std	-- (3)	-- (3)
Fast release	Std	Host	-- (2)	-- (2)
Floating point	Std	Std	Std	Std
Halt device	Std	Host	-- (2)	-- (2)
Interpretive execution (SIE)	--	--	Std	Host
Interval timer	Std	Std	--	--
Key-controlled storage protection	Std	Std	Std (4)	Std (4)
Limited channel logout	Std	Host	-- (2)	-- (2)
Monitoring	Std	Std	Std	Std
Multiprocessing:				
- CPU address identification	Std	Host	Std	Std
- CPU signaling and response	Std	Host	Std	Std
- Prefixing	Std	Host	Std	Std
- Shared main storage	Std	Host	Std	Std
- TOD clock synchronization	Std	Host	Std	Host
Page protection	--	--	Std	Std
PSW-key handling	Std	Std	Std	Std
Recovery extensions	Std	Host	--	--
Segment protection	Std	Std	-- (5)	-- (5)
Service signal	Std	Host	Std	Host
Sorting instructions	--	--	Std	Std
Storage key instruction extensions	Std	Std	Std	Std
Storage key instructions (ISK, SSK)	Std	Std	-- (4)	-- (4)
Storage-key 4K-byte block:				
- Single-key 4K-byte blocks	Std (6)	Std	Std	Std
- Storage-key exception control	Std	Std	-- (4)	-- (4)
System/370 extended facility:				
Non-MVS-dependent portion	Std	Std	Std	Std
System/370 I/O instructions	Std	Host	-- (2)	-- (2)
Test block	Std	Std	Std	Std
Time-of-day (TOD) clock	Std	Std	Std	Std
Tracing (ASN, branch, and explicit)	--	--	Std	Std
Translation:				
- Dynamic address translation:				
- 2K-byte page size	No	No	--	--
- 4K-byte page size	Std	Std	Std	Std
- 64K-byte segment size	Std	Std	--	--
- 1M-byte segment size	Std	Std	Std	Std
- Extended control (EC) mode	Std	Std	-- (1)	-- (1)
- Program-event recording (PER)	Std	Std	Std	Std
- Set-system-mask suppression	Std	Std	Std	Std
- Store status	Std	Std	Std	Std
Vector Facility	Opt	Opt	Opt	Opt
3033 extension:				
- Dual-address space (DAS)	Std	Std	Std (7)	Std (7)
- SIOF queuing	Std	Host	-- (2)	-- (2)
- Suspend and resume	Std	Host	-- (2)	-- (2)
31-bit IDAWs	Std	Host	Std	Std
31-bit real addressing	--	--	Std	Std

Figure 7-1. Features Dependent on Architectural Mode

Notes for Figure 7-1 on page 7-2:

--	Not defined in the principles of operation manual for this architectural mode, therefore, not implemented on the 3090.
Host	The design of the host programming determines whether or not this native function is simulated for the guest; direct interpretive execution does not occur.
No	Defined in the principles of operation manual for this architectural mode, but not implemented on the 3090.
Optional (Opt)	Implemented as a optional feature of the 3090 when operating in this architectural mode.
Standard (Std)	Implemented as a standard feature of the 3090 when operating in this architectural mode.

1 Operation in 370-XA mode is comparable to operation in EC mode of System/370.

2 Replaced by standard functions of the channel subsystem operating in 370-XA mode; channel program compatibility with System/370 is maintained.

3 Replaced by 31-bit real addressing.

4 The storage key instruction extensions provide the required function to manage the storage keys in 370-XA mode; System/370 instructions ISK, RRB, and SSK are not in 370-XA architecture.

5 Replaced by page protection.

6 Double-key 4K-byte blocks are not implemented.

7 Does not include dual address space (DAS) tracing; address space number (ASN) tracing provides a comparable function.

Programming Assist Feature	S/370 Native	S/370 (SIE) Guest	370-XA Native (Host)	370-XA (SIE) Guest
Control-switch assist	Std	--	-- (1)	-- (1)
Preferred-machine assist	Std	--	-- (1)	-- (1)
SIE assist	--	--	Std	Host
System/370 extended facility				
- MVS-dependent portion:				
- Four lock-handling instructions	Std	Std	Std	Std
- Six tracing instructions	Std	Std	-- (2)	-- (2)
- Fix Page instruction	Std	Std	--	--
- SVC Assist instruction	Std	Std	Std	Std
- Add Functional Recovery Routine instruction	Std	Std	Std	Std
- VM assist for MVS/370 assists	Std	Std	-- (1)	-- (1)
Virtual-machine assist	Std	--	-- (1)	-- (1)
VM assists for CPU timer	Std	--	-- (1)	-- (1)

Notes:

--	Not defined as a programming assist for this architectural mode, and therefore, not implemented on the 3090.
Host	The design of the host programming determines whether or not this native function is simulated for the guest; direct interpretive execution does not occur.
Standard (Std)	Implemented as a standard feature of the 3090 when operating in this architectural mode.
1	SIE provides an alternate means of supporting execution for one or more guest operating systems.
2	370-XA tracing provides a comparable function.

Figure 7-2. Programming Assist Features Dependent on Architectural Mode

Feature	Category
Channel group, 1st additional (8)	Optional (Model 200 only)
Channel group, 1st additional (16)	Optional (Model 400 only)
Channel group, 2nd additional (8)	Optional (Model 200 only)
Channel group, 2nd additional (16)	Optional (Model 400 only)
Channels (32)	Standard (Model 200 only)
Channels (64)	Standard (Model 400 only)
CPU retry	Standard
Data streaming	Standard
Error checking and correction	Standard
Expanded storage	Optional
High-speed buffer storage	Standard
I/O error alert	Standard
I/O power sequence control (Model 200)	Standard (For 1st to 64th control unit)
I/O power sequence control (Model 200)	Optional (For 65th to 128th control unit)
I/O power sequence control (Model 400)	Standard (For 1st to 128th control unit)
I/O power sequence control (Model 400) 1st additional	Optional (For 129th to 192nd control unit)
I/O power sequence control (Model 400) 2nd additional	Optional (For 193rd to 256th control unit)

Figure 7-3. Features Not Dependent on Architectural Mode

Basic Control Mode

Basic control (BC) mode provides a PSW format that is compatible with the PSW format of System/360.

Bimodal Addressing

Bimodal addressing permits 31-bit logical addressing, yet allows users to continue running System/370 problem programs, which use 24-bit logical addresses.

Branch and Save

Branch and save provides the Branch and Save instruction (BAS and BASR).

Byte-Oriented Operand

Byte-oriented operand allows storage operands of most unprivileged instructions to appear on any byte boundary without causing a specification exception and a program interruption. This feature applies to fixed-point, floating-point, and logical operands. It does not apply to

instruction addresses, privileged instructions, or channel command words (CCWs).

Channel Groups, Additional

Two additional groups of channels (8 each) are available for Model 200 for a total of 40 or 48 channels.

Two additional groups of channels (16 each) are available for the Model 400 for a total of 64 or 96 channels.

Channel Indirect Data Addressing

The addresses contained in channel command words (CCWs) in virtual storage must be translated by the system control program before execution. Channel indirect data addressing allows immediately adjacent areas of virtual storage to be mapped into nonadjacent areas of absolute storage.

Channel-Set Switching

Channel-set switching permits program-controlled switching of channel sets between two central processors so that if one central processor fails, either channel set may be assigned to the other central processor.

Channel Subsystem

The 370-XA dynamic subsystem queues I/O requests, selects from as many as four channel paths to any I/O device, and handles I/O busy conditions. Thirteen 370-XA I/O instructions are associated with the channel subsystem.

Model 400 is configured with a channel subsystem on each side. However, when single-image operation is in effect, the two channel subsystems operate as one 370-XA dynamic channel subsystem.

Channels

Thirty-two channels are standard on Model 200 and 64 channels are standard on Model 400. All channels can be assigned for block-multiplex operation, or as many as four channels (Model 200) or eight channels (Model 400) can be assigned for byte-multiplex operation.

Clear I/O

Clear I/O provides the clear I/O function in a channel when the privileged Clear I/O (CLRIO) instruction is executed. The clear I/O function causes a channel to discontinue its current I/O operation with an addressed I/O device by storing the status of the operation in the channel status word (CSW) and by making the associated subchannel available.

Command Retry

Command retry allows a subchannel to retry a command without causing an I/O interruption. The retry is initiated by a control unit.

Conditional Swapping

Conditional swapping makes available the Compare and Swap (CS) and Compare Double and Swap (CDS) instructions.

| Control Switch Assist

The control-switch assist enhances the functions of the preferred-machine assist by increasing the speed with which interruptions on CP owned channels are presented to a preferred virtual machine, and by allowing a preferred virtual machine to access certain control program (CP) DIAGNOSE codes. VM/SP-HPO releases 3.2 and up support control-switch assist.

CPU Retry

CPU retry automatically examines any instruction when an error occurs during the execution of the instruction. CPU retry usually attempts to reexecute the instruction.

CPU Timer and Clock Comparator

The CPU timer of each central processor is a high-resolution timer that causes an interruption whenever its value is negative. The interruption request is allowed by setting bit 21 in control register 0 and the external mask bit in the PSW.

The CPU timer measures central processor elapsed time and causes an interruption at the end of the period that is specified by the program. The timer is decremented when the central processor is executing instructions and during the wait state, but is not decremented when the central processor is in the stopped state. The program can initiate inspection of the CPU timer by using the Store CPU Timer (STPT) instruction and can

set the timer to a specific value by using the Set CPU Timer (SPT) instruction. The contents of the CPU timer are reset to 0 by initial CPU reset.

Note: When the TOD clock is in the stopped state or in the error state, the CPU timer is not decremented.

The clock comparator of each central processor provides for an interruption when the time-of-day (TOD) clock reaches a value specified by the program. The interruption is allowed when the central processor sets bit 20 in control register 0 and the external mask bit in the PSW.

The format of the clock comparator is the same as that of the TOD clock. A clock-comparator interruption is an external interruption. The program can initiate inspection of the clock comparator by using the Store Clock Comparator (STCKC) instruction and can set it by using the Set Clock Comparator (SCKC) instruction. The contents of the clock comparator are reset to 0 by an initial CPU reset.

Note: When the TOD clock is in the stopped state or in the error state, the clock comparator is not operating.

Data Streaming

Data streaming is available on all block-multiplexer channels. It permits higher data rates (as many as 3.0 megabytes per second) and longer cable lengths. Data streaming is initiated by the control unit. The channel subsystem permits the intermixed attachment of data-streaming and non-data-streaming devices on the same channel.

Error Checking and Correction

Data paths between expanded storage (if installed) and central storage and between central storage and the channels and central processors are checked using either parity or error checking and correction.

Error checking and correction (ECC) code bits are stored with the data in the central storage and in the expanded storage data arrays. ECC codes apply to data stored in and fetched from central storage and expanded storage; single-bit and multiple-bit error detection are performed in both central storage and expanded storage. Single-bit error correction takes place in central storage while both single-bit and double-bit error correction take place in expanded storage.

Expanded Storage

Expanded storage is an optional high-speed, high-capacity storage that transfers 4K-byte pages to and from central storage. Expanded storage is available in 64M-byte increments to a maximum of 128M bytes for Model 200, and in 128M-byte increments to a maximum of 256M bytes for Model 400.

Extended-Precision Divide

Extended-precision divide provides the Divide (DXR) instruction for extended-precision floating-point operands.

Extended-Precision Floating Point

Extended-precision floating point provides seven floating-point instructions that use the extended-precision format (a signed 7-bit characteristic and a 28-digit fraction).

Extended Real Addressing

Extended real addressing permits the addressing of real storage in excess of 16M bytes. The system control program uses extended real addressing for locating user programs and portions of the system control program in central storage at real addresses to 64M bytes. Extended real addressing does not affect virtual addressability, which may not exceed 16M bytes.

Fast Release

Fast release provides the start-I/O-fast-release function on a channel when the Start I/O Fast Release (SIOF) instruction is executed. This function provides for early release of the central processor that executes the instruction. Fast release occurs before the device-selection procedure is completed, thereby reducing the central processor delay associated with the operation.

Floating Point

Floating point provides the floating-point instructions and the floating-point registers. In System/370, floating point combined with the commercial instruction set is sometimes referred to as the System/370 universal instruction set.

Halt Device

Using the privileged Halt Device (HDV) instruction, the halt-device function signals the addressed I/O device to terminate its current I/O operation.

High-Speed Buffer Storage

High-speed buffer storage in each central processor satisfies many storage fetch requests, making the effective storage access time much shorter than the actual central storage cycle time. (For more information, see "Buffer Control Element" in Chapter 3.)

Interpretive Execution

The interpretive execution facility is used by the VM/XA Systems Facility and provides hardware support for several areas of virtual machine operation, such as interval timer operation, prefixing, address translation, and privileged instruction handling. This facility provides the SIE instruction (with interception format 2 installed), which the VM/XA Systems Facility uses to dispatch all virtual machines.

Interval Timer

The interval timer of each central processor provides external interruptions on a program-controlled basis. The value stored at a specified storage location is automatically decremented by 1 in bit position 23 every 3.33 milliseconds. The program receives an external interruption request when the interval timer decrements from 0 to a negative value. (Bit 7 of the PSW and bit 24 of control register 0 must be on.) The range of the interval timer is approximately 15.5 hours.

Note: When the central processor's TOD clock is in the stopped or error state, the interval timer is not operating.

I/O Error Alert

I/O error alert permits a channel to be alerted when a malfunction affects the ability of a control unit to continue operating.

I/O Power Sequence Control

I/O power sequence control permits the 3090 to sequence power (for power on or power off) for as many as 64 control units for Model 200 and 128 control units for Model 400. If more control units are needed, additional I/O power sequence control features are optionally available to provide power-on and power-off control for 64 more control units. One I/O power sequence control feature (64 additional control units) may be installed for Model 200; one or two I/O power sequence control features (for a total of 192 or 256 control units) may be installed for Model 400.

Key-Controlled Storage Protection

Key-controlled storage protection prevents unauthorized access to information in central storage. Key-controlled storage protection includes both store protection and fetch protection. If store protection is violated, data is not stored into the protected area; if fetch protection is violated, data is not retrieved from the protected area. When a violation is recognized, a program interruption occurs. (See "Central Storage" in Chapter 3 for more information.)

Limited Channel Logout

Limited channel logout provides 4 bytes of channel-status information for model-independent recovery from channel errors.

Monitoring

Monitoring provides a means of selectively recording designated events in the execution of a program. This facility is implemented by the Monitor Call (MC) instruction.

Multiprocessing

With two (Model 200) or four (Model 400) central processors, the multiprocessing feature permits a multiprocessing configuration. Multiprocessing provides CPU address identification, CPU signaling and response, prefixing, shared main storage, and TOD clock synchronization.

CPU Address Identification

CPU address identification provides an address by which each of the central processors can be identified by the Signal Processor (SIGP) instruction. It also provides new external interruption conditions and the Store CPU Address (STAP) instruction, by which the system control program can determine the address of a central processor.

CPU Signaling and Response

CPU signaling and response provides for communication among the central processors. This feature provides the Signal Processor (SIGP) instruction and the mechanism to interpret and act on several order codes, such as sense, stop, and restart.

Prefixing

For each central processor, prefixing provides a means of assigning real addresses 0 through 4095 to different 4K-byte blocks of central storage. One area of central storage (represented by a single contiguous range of absolute addresses) is assigned to each central processor.

Shared Main Storage

Shared main storage permits all central processors to have access to common main storage locations.

TOD Clock Synchronization

TOD clock synchronization provides a uniform appearance to a clock synchronization program in all 3090 Processor Complexes, allowing the program to be independent of the actual number of TOD clocks and central processors in a configuration. It includes a TOD clock synchronization control bit in control register 0.

Page Protection

Page protection provides protection against improper storing by controlling access to virtual storage by using the page protection bit in each page table entry.

| Preferred Machine Assist

| Preferred machine assist permits a single MVS/SP virtual-equals-real (V=R) virtual machine operating under VM/SP-HPO to operate with a minimum of simulated instruction execution. This allows the MVS/SP virtual machine to achieve near native performance. With preferred machine assist, any MVS/SP release that supports more than 16M bytes of real storage can use real storage above 16M bytes when MVS/SP is operating as a V=R virtual machine.

PSW-Key Handling

PSW-key handling provides the Set PSW Key from Address (SPKA) and Insert PSW Key (IPK) instructions.

Recovery Extensions

Recovery extensions consist of:

- The clear channel function in a channel, which can be used to perform an I/O system reset in a channel when the Clear Channel (CLRCH) instruction is executed.
- Machine-check extensions, which include a machine-check external damage-code validity bit and which provide a detailed indication of the cause of external damage.
- Limited channel logout extensions, which consist of two additional logout bits, to indicate whether the I/O interface is operative and whether the logout is valid.

Segment Protection

Segment protection provides protection against improper storing by controlling access to virtual storage by using the segment protection bit in each segment-table entry.

Service Signal

Service signal provides an external interruption that is used by the 3092 Processor Controller to signal information to the system control program.

SIE Assist

The SIE assist improves the performance of V=R preferred guests running under the VM/XA Systems Facility. Certain I/O instructions and associated I/O interruptions can be handled in the interpretive execution mode, for both System/370 and 370-XA guests, if associated with devices dedicated to the guest.

Sorting Instructions

Sorting instructions are used by the IBM Program Product DFSORT (Data Facility Sort), Release 7 and later, running under MVS/XA. The sorting instructions are used when sorting fixed-length records using the block-set sorting technique by the program DFSORT (Release 7 and later).

Storage Key Instruction Extensions

The storage key instruction extensions provide the Set Storage Key Extended (SSKE), Insert Storage Key Extended (ISKE), and Reset Reference Bit Extended (RRBE) instructions, which provide 31-bit addresses and operate on the storage key associated with each 4K-byte block of storage.

Storage Key Instructions

The storage key instructions Set Storage Key (SSK) and Insert Storage Key (ISK) allow initialization and inspection of the storage key associated with each block of storage that is available in the configuration.

Storage-Key 4K-Byte Block

Storage-key 4K-byte block allows a single key to be associated with each 4K-byte block of storage and, in S/370 mode, provides the storage-key exception control bit in control register 0.

System/370 Extended Facility

The non-MVS-dependent portion of the System/370 extended facility consists of:

- Low-address protection, which improves system integrity by providing special protection for storage (at fixed storage addresses 0 through 511) that is vital to the system control program.
- Invalidate Page Table Entry (IPTE) instruction and the common-segment bit, which increase the efficiency of dynamic address translation.
- Test Protection (TPROT) instruction, which performs tests for potential protection violations without causing program interruptions for protection exceptions.

The MVS-dependent portion of the System/370 extended facility consists of:

- Service Call (SVC) Assist instruction, which improves central processor performance by reducing the time needed to enter MVS supervisory services

- Fix Page instruction, Add Functional Recovery Routine (FRR) instruction, six tracing instructions, and four lock-handling instructions, which improve central-processor performance

System/370 I/O Instructions

The I/O instructions used in S/370 mode are:

- Clear Channel (CLRCH)
- Clear I/O (CLRIO)
- Halt Device (HDV)
- Halt I/O (HIO)
- Resume I/O (RIO)
- Start I/O (SIO)
- Start I/O Fast Release (SIOF)
- Store Channel ID (STIDC)
- Test Channel (TCH)
- Test I/O (TIO)

Test Block

Test block provides the Test Block (TB) instruction for testing the usability of a 4K-byte block of central storage.

Time-of-Day Clock

The time-of-day (TOD) clock for each central processor provides a consistent measurement of elapsed time that can be used for indicating the time of day. The TOD clock for each central processor is initialized by the Set Clock (SCK) instruction by a central processor.

- Bit 51 increments at 1-microsecond intervals.
- Bits 52-55 are monotonic to ensure 1-microsecond counting in bit 51.
- Bits 61-63 contain the central processor address.

Tracing

Tracing provides three aids for problem-program analysis:

- Address-space-number (ASN) tracing
- Branch tracing
- Explicit tracing

Translation

Translation includes the following features:

- Dynamic address translation
- Extended control (EC) mode
- Program-event recording (PER)
- Set-system-mask suppression
- Store status

As part of these features, translation also provides the following instructions:

- Load Read Address (LRA)
- Purge Translation Lookaside Buffer (PTLB)
- Reset Reference Bit (RRB)
- Store Then AND System Mask (STNSM)
- Store Then OR System Mask (STOSM)

Dynamic Address Translation

Dynamic address translation (DAT) provides hardware translation of virtual addresses to real addresses during program execution. DAT supports real storage sizes for as many as 64M bytes for Model 200 and for as many as 128M bytes for Model 400. The 3090 uses 4K-byte pages and either 64K-byte segments or 1M-byte segments (in S/370 mode), or 1M-byte segments only (in 370-XA mode).

A guest virtual machine in S/370 mode using interpretive execution can use the 1M-byte segment size.

Extended Control Mode

When the 3090 operates in extended control (EC) mode, virtual storage and high-speed DAT are available.

Program-Event Recording

Program-event recording (PER) aids in debugging programs. During program execution, PER can monitor the following actions:

- Successful branches
- Alteration of general registers
- Instruction fetches from a specified storage area
- Alteration of a specified storage area

Set-System-Mask Suppression

Set-system-mask suppression permits suppression of execution of the Set System Mask (SSM) instruction and provides the special-operation program interruption code.

Store Status

Store status is an operator-initiated function that places the contents of the current PSW and the program-addressable registers in permanently assigned locations within the first 512 bytes of absolute storage. Store status also includes a non-initializing manual reset function.

| Vector Facility

The vector facility is optional for each of the central processors of the 3090 Processor Complex Models 200 and 400. Central processors with the optional vector facility provide significantly increased levels of performance for many compute-intensive engineering and scientific applications.

| Virtual Machine Assist

Virtual-machine assist (VMA), which is a programming assist for VM/SP, directly executes 15 virtual-machine instructions (including the ISKE, SSKE, and RRBE instructions) and validates page-table entries in the shadow tables. VMA improves performance on virtual-storage systems operation under VM/SP by reducing the amount of time VM/SP spends in the real supervisor state. The reduction is achieved by emulation (instead of software simulation) of certain privileged operation codes used by the virtual-storage (guest) control program.

VM Assists for the CPU Timer

VM assists for the CPU timer permit a central processor to directly execute the Set CPU Timer (SPT) and Store CPU Timer (STPT) instructions for a virtual machine operating under VM/SP.

3033 Extension

The 3033 extension provides the following facilities to the 3090:

- Dual-address space
- Start-I/O-fast queuing
- Suspend and resume

All three facilities are supported in S/370 mode by MVS/SP Version 1 Release 3; dual-address space is supported in 370-XA mode by MVS/SP Version 2.

Dual-Address Space

Dual-address space aids communication between virtual address spaces. It provides:

- Twelve additional instructions
- Two address spaces for immediate use by a program
- Means of changing to other virtual address spaces
- A table-based subroutine linkage
- The use of multiple access keys for key-controlled protection by problem programs
- Aids for problem-program analysis (S/370 mode only)

In 370-XA mode, the tracing facility provides an alternative set of aids.

Start-I/O-Fast Queuing

Start-I/O-fast queuing allows a Start I/O Fast Release (SIOF) instruction to complete execution independent of device selection or a channel-busy condition. Control-unit or device busy conditions encountered subsequent to execution of an SIOF instruction cause the I/O operation to remain pending until facilities are available for initiation of the operation at the device.

Suspend and Resume

Suspend and resume provides:

- The suspend flag in the channel command word (CCW), which indicates that execution of a channel program is to suspended
- A channel address word (CAW) bit that controls whether the CCW's suspend flag should cause suspension of execution of a channel program
- A channel status word (CSW) bit that indicates that execution of a channel program has been suspended
- The Resume I/O (RIO) instruction, which causes resumption of execution of a suspended channel program

31-Bit Indirect Data Address Word

The 31-bit indirect data address word (IDAW) extends the size of the address field in IDAWs to 31 bits.

31-Bit Real Addressing

Thirty-one bit real addressing ensures that certain fields contain 31-bit real addresses regardless of the setting of the addressing-mode control bits in the PSW.

Appendix A. 3090 Deviations

The following information describes 3090 deviations from the *IBM System/370 Principles of Operation* and the *IBM System/370 Extended Architecture Principles of Operation.*

Concurrent Indication of PER Events with Operand-Access Exceptions

(The 3090 deviates from both S/370 and 370-XA Principles of Operation.)

Storage alteration PER events may be indicated for execution of the instructions Edit, Edit and Mark, and Translate when an operand-access exception is encountered that nullifies or suppresses instruction execution.

Protection Violation Instead of Delayed Access Exception

(The 3090 deviates from both S/370 and 370-XA Principles of Operation.)

The S/370 and 370-XA Principles of Operation permit considerable extent of unpredictability when a valid and attached DAT table entry is changed and the entry is used for translation before the TLB is cleared of copies of that entry. The definition permits changes to all of those result fields that are not protected. Changes can occur, for example, to the condition code, operands due to be changed in registers, and to those portions of the operands due to be changed in storage for which no access exception exists.

The 3090 deviates from the architecture in that:

Protection exceptions that occur after the initial pretest are ignored, the storing for a store-type reference takes place, and no interruption occurs. This includes protection exceptions due to key-controlled protection, page protection, and segment protection.

Glossary of Terms and Abbreviations

auto-vectoring. Occurs when VS FORTRAN Extended source code is automatically compiled to contain object code with vector instructions.

abend. Abnormal end of task or of processing.

acronym. A special type of abbreviation in which the characters chosen to abbreviate the word or words deliberately spell a word (as in RAM, COBOL, or BASIC).

address. An identification of a storage location or an I/O device.

address translation. See *dynamic address translation.*

analysis routine (AR). A routine that uses error records to indicate the field-replaceable unit (FRU) or FRU group that probably caused the error.

AR. Analysis routine.

ASN. Address space number.

BAS. Branch and Save instruction.

BASR. Branch and Save instruction.

BC. Basic control mode.

BCE. Buffer control element.

bit. Binary digit.

BOC. Battery-operated clock.

bpi. Bit per inch.

cache. A high-speed buffer.

CAW. Channel address word (S/370).

CC. Condition code.

CCC. Channel control check.

CCE. Channel control element.

CCW. Channel command word.

CDC. Channel data check.

CDS. Compare Double and Swap instruction.

central storage. Includes both main storage (programs and data) and the hardware system area (not addressable by programming). Available to the channel subsystem and all central processors.

channel. Each channel in the channel subsystem controls an I/O interface between the channel control element and the attached control units.

channel control element (CCE). The channel control element in the channel subsystem.

channel subsystem (CSS). The channel subsystem is responsible for all I/O operations.

CHPID. Channel path identifier.

CLRCH. Clear Channel (S/370 I/O instruction).

CLRIO. Clear I/O (S/370 I/O instruction).

compute intensive. Characterized by high central processor utilization.

console. A logical device that is used for communication between the user and the system. See *display station.*

consoles. See *monitor consoles, operator console, programming support console, service console, system console.*

control, operator. Any control (hardware or microcode) that can be used to communicate with the processor complex. Controls can include switches, pushbuttons, function keys, commands, and display frames.

CP. Central processor (as in CP1, CP2).

CPU. Central processor.

CRW. Channel report word (370-XA).

CS. Compare and Swap instruction.

CSCH. Clear Subchannel (370-XA I/O instruction).

CSE. Control storage element (CP).

CSS. Channel subsystem.

CSW. Channel status word.

CTCA. Channel-to-channel adapter.

CU. Control unit.

DACB. Device address control block.

DAT. Dynamic address translation.

display station. A physical device that can be used as multiple logical consoles. See *console.*

DXR. Divide instruction.

dyadic processor. A two-way multiprocessor that uses two central processors for instruction execution while sharing central storage and channels.

dynamic address translation (DAT). The conversion of virtual addresses to real addresses immediately before the address is used, allowing the use of virtual addresses in instructions and commands.

EC. Extended control mode.

ECC. Error checking and correction.

ECL. Emitter-coupled logic.

ECW. Extended control word (370-XA).

EE. Execution element (CP).

element. A major part of a component (for example, the buffer control element) or a major part of the processor complex (for example, the system control element).

error checking and correction (ECC). Hardware that automatically corrects all single-bit errors and detects all double-bit errors and most triple-bit errors. The error checking and correction hardware in expanded storage corrects all single-bit errors and all double-bit errors and detects all triple-bit errors.

ESW. Extended status word (370-XA).

expanded storage. Optional integrated high-speed storage that transfers 4K-byte pages to and from central storage.

facility. Hardware and software that provide useful capabilities for humans (as in an operator facility or a maintenance service facility).

FCC. Federal Communications Commission.

FP. Floating point.

FPR. Floating-point register.

FRR. Functional Recovery Routine instruction.

FRU. Field-replaceable unit.

ft. (1) Foot. (2) Feet.

G-byte. 1 073 741 824 bytes.

gigabyte. 1 073 741 824 bytes.

GR. General register (CP).

guest. In interpretive execution mode, the interpreted or virtual machine as opposed to the real machine (host).

hardware system area (HSA). A logical area of central storage that is used to store microcode, instructions, and control information (not addressable by application programs).

HDV. Halt Device instruction (S/370).

hex. Hexadecimal.

high-speed buffer. A 64K-byte cache (one for each central processor).

HIO. Halt I/O (S/370 I/O instruction).

host. In interpretive execution mode, the real machine as opposed to the virtual or interpreted machine (the guest).

HSA. Hardware system area.

HSCH. Halt Subchannel (370-XA I/O instruction).

ID. (1) Identifier. (2) Identification.

IDAW. Indirect data address word.

IE. Instruction element.

IFCC. Interface control check.

IML. Initial microprogram load.

initialization. To set counters, switches, addresses, latches, or storage contents to 0 or to other starting values at the beginning of, or at the prescribed points in, a computer program or process.

I/O. Input/output.

I/O Configuration Program (IOCP). Defines for the central processors all of the I/O devices and all of the available channel paths.

I/O interface. The I/O interface connects channels and control units for the exchange of signals and data.

IOCDS. I/O configuration data set.

IOCP. I/O Configuration Program.

IOPD. (1) I/O problem determination. (2) I/O Problem Determination frame.

IOTA. Input/output transaction area.

IPK. Insert PSW Key instruction.

IPL. Initial program load.

IPTE. Invalidate Page Table Entry (370-XA instruction).

ISK. Insert Storage Key instruction

ISKE. Insert Storage Key Extended instruction.

K-byte. 1024 bytes.

kilobyte. 1024 bytes.

LCL. Limited channel logout (S/370).

LCU. Logical control unit (370-XA).

limited channel logout (LCL). An error record containing detailed information about an error affecting an I/O operation.

logout. Log data that has been collected, formatted, and recorded.

LRA. Load Read Address instruction.

M-byte. 1 048 576 bytes.

MC. Monitor Call instruction.

MCCU. IBM 3088 Multisystem Channel Communication Unit.

MCIC. Machine-check interruption code.

megabyte. 1 048 576 bytes.

MFLOPS. Millions of floating-point operations per second.

MHz. Megahertz.

microsecond. One millionth of a second.

modem. Modulator-demodulator.

monitor consoles. Optional logical displays that are used to monitor the service or system consoles. Each monitor console can be assigned to any of the physical displays attached to the 3092.

MSCH. Modify Subchannel (370-XA I/O instruction).

multiplexing. The ability of the channel and the device to disconnect and reconnect during an operation.

MVS/SP. Multiple Virtual Storage/System Product.

nanosecond (ns). One thousandth of a microsecond.

ns. Nanosecond.

OLTS. Online test system.

operator console. Required display that is channel attached to the processor unit to provide communication with the system control program.

operator control. Any control (hardware or microcode) that can be used to communicate with the processor complex. Controls can include switches, pushbuttons, function keys, commands, and display frames.

PA. Program area (of central storage).

PCDU. Power and coolant distribution unit.

PER. Program-event recording.

port. An access point for data entry or exit.

processor complex. A configuration comprising the:

- Processor unit
- Processor controller
- System display
- Service display
- Power and coolant distribution unit
- Power units

processor controller. Provides support and diagnostic functions for the central processors.

programming support console. Logical device used as a data bank access console. The programming support console can be assigned to any of the physical displays attached to the 3092 Processor Controller.

PSW. Program status word.

PTLB. Purge Translation Lookaside Buffer instruction.

RAS. Reliability, availability, and serviceability.

RIO. Resume I/O (S/370 I/O instruction).

RRB. Reset Reference Bit instruction.

RRBE. Reset Reference Bit Extended instruction.

RSCH. Resume Subchannel (370-XA I/O instruction).

RSF. Remote support facility.

S/370. System/370 mode.

SAD. System activity display.

SCE. System control element.

SCH. Subchannel.

SCK. Set Clock instruction.

SCKC. Set Clock Comparator instruction.

SCP. System control program.

service console. Logical device used by service personnel to maintain the processor complex and to isolate failing FRUs. The service console can be assigned to any of the physical displays attached to the 3092 Processor Controller.

service display. A required IBM 3180 Display Station that can be attached to a port on the active side of the processor controller, and that can be switched to a control unit on a channel of the 3092 Processor Controller for online test program use.

SIE. Start Interpretive Execution (370-XA instruction).

SIGP. Signal Processor instruction.

single channel service (SCS). The capability of running diagnostic tests on a single channel while the other channels are being used by the customer.

SIO. Start I/O (S/370 I/O instruction).

SIOF. Start I/O Fast Release (S/370 I/O instruction).

SP-HPO. System Product-High Performance Option.

SPKA. Set PSW Key from Address instruction.

SPT. Set CPU Timer instruction.

SSCH. Start Subchannel (370-XA I/O instruction).

SSK. Set Storage Key instruction.

SSKE. Set Storage Key Extended instruction.

SSM. Set System Mask instruction.

STAP. Store CPU Address instruction.

STCKC. Store Clock Comparator instruction.

STCPS. Store Channel Path Status (370-XA I/O instruction).

STCRW. Store Channel Report Word (370-XA I/O instruction).

std. Standard.

STIDC. Store Channel ID (S/370 I/O instruction).

STIDP. Store CPU ID instruction.

STNSM. Store Then AND System Mask instruction.

storage key. A control field associated with a defined block of storage that protects that block of storage from unauthorized access and change.

STOSM. Store Then OR System Mask instruction.

STPT. Store CPU Timer instruction.

subchannel. The channel subsystem facilities required for sustaining a single I/O operation.

SVC. Service Call instruction.

system. The processor complex and its attached and configured I/O and communication devices.

system console. A logical device used for the operation and control of hardware functions (for example, IPL, alter/display, and reconfiguration). The system console can be assigned to any of the physical displays attached to the 3092 Processor Controller.

system control element (SCE). Handles the transfer of data and control information associated with storage requests between the elements of the processor complex.

system display. A required 3180 Display Station that can be attached to a port on the active side of the 3092 Processor Controller.

TB. Test Block instruction.

TCH. Test Channel (S/370 I/O instruction).

TCM. Thermal conduction module.

thermal conduction module (TCM). A field-replaceable unit containing multiple logic chips.

TIO. Test I/O (S/370 I/O instruction).

TLB. Translation lookaside buffer. (Directory lookaside buffer in the CP.)

TOD. Time of day.

TPROT. Test Protection instruction (370-XA).

TSCH. Test Subchannel (370-XA I/O instruction).

UCW. Unit control word.

V=V. Virtual equals virtual.

Vector facility. The vector facility is optional for the central processors of the 3090 Processor Complex Models 200 and 400. Central processors with the optional vector facility provide significantly increased levels of performance for many compute-intensive engineering and scientific applications.

VF. Vector facility.

VM/SP. Virtual Machine/System Product.

VM/XA. Virtual machine/extended architecture.

VSE. Virtual storage extended

370-XA. System/370 extended architecture.

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Bibliography

The following publications provide additional information about 3090 Processor Complex functions and operations:

GA22-6974 *IBM System/360 and System/370 I/O Interface Channel to Control Unit Original Equipment Manufacturers' Information*

GA22-7000 *IBM System/370 Principles of Operation*

GA22-7001 *IBM System/370 System Summary: Processors*

GA22-7002 *IBM System/370 Input/Output Configurator*

GA32-0039 *IBM Input/Output Device Summary*

GC22-7064 *IBM Input/Output Equipment Installation Manual—Physical Planning for System/360, System/370, and 4300 Processors*

GC22-7074 *IBM System/370 3090 Processor Complex Installation Manual—Physical Planning*

SA22-7085 *IBM System/370 Extended Architecture Principles of Operation*

SA22-7095 *IBM System/370 Extended Architecture Interpretive Execution*

SA22-7120 *IBM 3090 Processor Complex Channel Characteristics and Configuration Guide*

SA22-7121 *IBM 3090 Processor Complex Functional Characteristics*

SC38-0038 *3090 Processor Complex: Input/Output Configuration Program User's Guide and Reference*

SC38-0039 *3090 Processor Complex: Operator Messages for the System Console*

SC38-0040 *3090 Processor Complex: Operator Controls for the System Console*

SC38-0041 *3090 Processor Complex: Operator Tasks for the System Console*

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Numerics

IBM 3090 Processor Complex Functional Characteristics

Order No. SA22-7121-1

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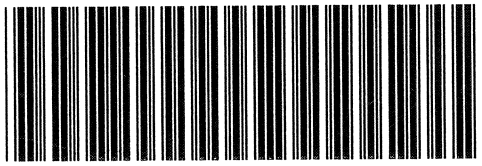


IBM®

New technology providing new opportunities

S/390 Parallel Enterprise Server

Highlights

Lower your cost of computing with S/390® CMOS general purpose processors

Reduce your operating costs and increase performance because complementary metal oxide semiconductor (CMOS) air-cooled processors lower your consumption of energy, reduce the footprint and lower maintenance costs.

Increase capacity easily with granularity offered through the S/390 Parallel Enterprise Server family

Use parallel sysplex to share data, configure for continuous availability and take advantage of improved software pricing while increasing capacity with granular increments.

Use client/server and keep the classic strength and power of S/390

New features such as the Open Systems Adapter 2 deliver connectivity to Ethernet, Token Ring and FDDI Local Area Networks.

Migrate to IBM's advanced technology

S/390 CMOS processors are a natural replacement for 4381, 308X, 3090™, many ES/9000™ and "plug compatible" systems. S/390 CMOS technology delivers high performance in a small package.

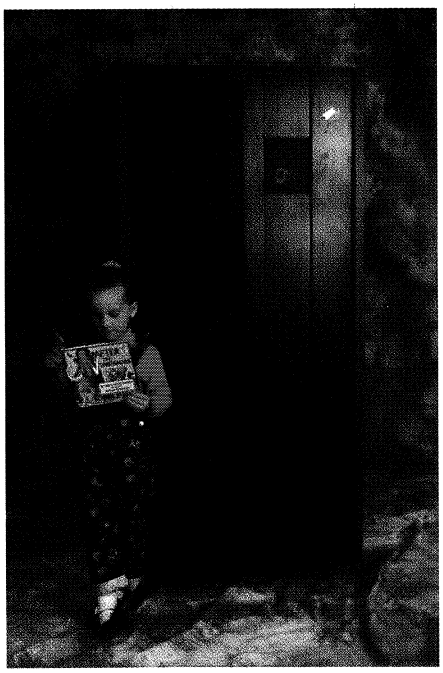
The time is now

Driving down the cost of computing, additional user demands, greater performance requirements, centralization of applications and business growth may cause you to consider processor alternatives. Now there's a new processor choice from IBM that takes you beyond used equipment, 4381, 308*x*, 3090 and "plug compatible machines." The S/390 Parallel Enterprise Server is a solid foundation for growth into the next century.

Vosper Thornycroft, a large ship building company in the United Kingdom, increased its computing power with the Parallel Enterprise Server and is positioned to take advantage of an open, distributed and integrated environment.

"We have solved our response time problems and are finishing our batch work in half the time. In addition, the new system has provided us with the framework we need to move forward with our plans for more open, distributed systems with full integration and shared data while retaining the benefits of a mainframe environment."

Steve Tamblyn, IT Manager



The 9672 Parallel Enterprise Server will grow with your business needs.

Twelve new models

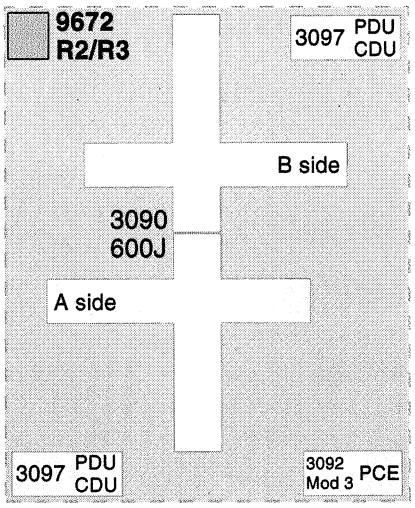
S/390 Parallel Enterprise Server processors include twelve new models with up to ten air-cooled IBM CMOS processors which are supported by VSE/ESA™, VM/ESA®, MVS/ESA™ and TPF™. These new models are upgradeable from the original 9672 "R1" models. You get application compatibility in a smooth upgrade that can reduce your cost of computing while improving performance.

Total economy
There are many reasons why upgrading to the S/390 Parallel Enterprise Server may be your most economical choice, even in the short term. The most obvious is power consumption. Thanks to the inherent efficiency of CMOS technology, replacing an air-cooled 9121-320 with a new 9672-R12 S/390 Parallel Enterprise Server can cut your energy cost by up to 85%, while increasing performance 10 to 30%. Similarly, replacing a water-cooled 3090-600J with a seven-way 9672-R73 can reduce your energy bill 97% and give you up to 20% more performance.

At the same time, the 9672-R12 Parallel Enterprise Server can cut the 9121-320's maintenance costs. The seven-way takes 94% less floor space than the 3090 600J, and can cost 65% less to maintain. Taken together, savings in energy and maintenance can add up to $2,000 a month when replacing the 9121-320 and over $15,000 a month when replacing the 3090. (Of course your savings will vary with local energy costs and other factors. Your IBM representative will be glad to help you calculate the savings in your particular situation.)

And these are just the direct savings
One of the many advanced functions the S/390 Parallel Enterprise Server delivers is hardware-assisted data compression. You can use this feature to extend the capacity of your communications and DASD devices, increasing the return on your investment in these subsystems.

Plus, there are productivity benefits built into the S/390 Parallel Enterprise Server's hardware management console. It features an easy-to-learn/easy-to-use graphical user interface that displays real-time status using color icons. System management becomes simpler, exceptions can be picked up sooner and your operator can work more efficiently than before.



The Parallel Enterprise Server requires 16 times less floor space than a 600J and consumes 28 times less energy.

Memphis City Schools, the 19th largest school district in the United States, replaced a 3090-200E with a Parallel Enterprise Server to facilitate integration of a client/server environment.

"Operating costs were drastically reduced by moving to an air-cooled processor and its lower environmentals."

Linda Mainord, Director, Technology Special Projects

Powerful features
Your S/390 Parallel Enterprise Server solution includes many advanced functions.

For example, PR/SM™ (Processor Resource/Systems Manager™) enables you to logically divide your processor for increased operational efficiency. PR/SM has been continually enhanced since its introduction over seven years ago. The S/390 Parallel Enterprise Server supports up to ten logically isolated system images.

These new models support up to 192 ESCON® (Enterprise Systems Connection Architecture®) channels. This allows you to evolve your data center to IBM fiber optic connectivity for greater flexibility and availability. ESCON connectivity allows you to attach devices up to 63 kilometers away. The S/390 Parallel Enterprise Server also supports up to 96 parallel channels or a combination of parallel and ESCON channels.

Gateway to the open world
The S/390 Open Systems Adapter 1 (OSA 1) was introduced in November of 1994, enabling enterprise-wide open computing. OSA 1 is a fully integrated S/390 hardware feature, delivering connectivity to Ethernet, Token Ring and Fiber Distributed Data Interface (FDDI) Local Area Networks (LANs). OSA 1 provides this direct LAN connectivity to Systems Network Architecture/ Advanced Peer to Peer Networking (SNA/APPN®), Transmission Control Protocol/Internet Protocol (TCP/IP) and IPX clients from S/390 server resources.

You also benefit from the offloading of the TCP/IP protocol stack from the S/390 server to OSA 1. Support is also provided for disk and print serving and data distribution using LANRES/MVS and Network File Serving using LAN Server for MVS.

OSA 1 and the S/390 Open Systems Adapter 2 (OSA 2) are complementary features and can be directly connected to high performance workstations, intelligent hubs, routers, bridges and LAN backbones. OSA 1's enhanced functions necessitated unique packaging, requiring a dedicated cage for the features.

The OSA 2 feature is plugged directly into a standard cage. The OSA 2 card is a single "book" package that is plugged into an I/O slot. This makes OSA 2 an integral component of the system, enabling convenient LAN attachment.

OSA 2 supports TCP/IP passthru in the MVS and VM environments and SNA/APPN passthru in the MVS environment using ACF/VTAM. All processing is performed on the S/390 server (passthru). TCP/IP and SNA/APPN applications can share access to an OSA 2 and can access the same LAN port. This delivers direct access to Ethernet, Token Ring and FDDI LANs in a dynamic fashion.

Share data and reduce software costs

If you anticipate continued growth or wish to have your processor take advantage of a Parallel Sysplex environment, all 9672 "R" models support coupling links. Using coupling links, you can couple the 9672-R with existing 511- and 711-based S/390 processors to configure for continuous availability, share data, take advantage of improved software pricing and grow to the largest S/390 single system image.

Increase your profitabilty and productivity through availability

The purpose of corporate computing is to enhance the productivity and profitability of the organization. To maximize this goal, the S/390 Parallel Enterprise Server comes with several standard availability features.

You can eliminate most scheduled outages for channel repair because concurrent channel maintenance enables the replacement of channel cards while the system is active. You can also dynamically alter the I/O configuration without a power-on reset or initial program load. In addition, a failing power supply can be bypassed so you can postpone replacement until regularly scheduled service.

On the new Parallel Enterprise Servers the power subsystem has been extensively redesigned and offers independent dual power feeds. Each feed is electrically isolated and enables redundant power paths. You may elect to provide dual electrical service (two sources of power) to the server, further minimizing any outages resulting from single path power interruptions.

To further reduce any power outages, a Local Uninterruptible Power Supply (Local UPS), Machine Type 9910 is available for the server. This unit provides over five minutes of power reserve in the event of extended power line disturbances.

Another example of fault tolerance can be found in processor storage. The S/390 Parallel Enterprise Server uses IBM memory card technology that detects memory problems and allocates backup memory at power on and reset.

In addition, S/390 Parallel Enterprise Servers feature automated problem diagnosis and isolation tools.

What does this add up to?

The result for you could be the best of several worlds: users delighted with their IS support, corporate management pleased with dramatically reduced computing costs and a data center with the flexibility to leverage new technology, control costs and provide enterprise-wide computing power for today and the future.

"We are immensely pleased with the CMOS technology and subsequently have eliminated all of our CICS™ and DB2® performance bottlenecks. We have only scratched the surfaces in our abilities to exploit this technology."

John Pumphrey, Loudon County Virginia Chief of Technical Operations

Advanced features:

- ESA/390 architecture
- Hardware Assisted Data Compression
- Asynchronous Data Mover Facility
- Open Systems Adapter 1 (OSA 1)
- Open Systems Adapter 2 (OSA 2)*
- Sysplex Timer Support

PR/SM features

- Processor Resource/Systems Manager (PR/SM)
- 10 PR/SM Partitions Supported
- Dynamic I/O Reconfiguration Management
- Partition Weight Management
- LPAR Definitions Retained
- LPAR Preferred Path
- LPAR Management Time Reporting
- Resource Capping
- ESCON Multiple Image Facility (EMIF)
- Dynamic Storage Reconfiguration 1 (DSR 1)
- Logical CP Vary On/Off

ESCON features

- ESCON Channels, 17 MB/second
- ESCON CTC Basic Mode

Performance features

- DB2 Sort Assist
- SIE Assist
- Move Page
- Enhanced Move Page
- Hiperbatch
- Scalar Square Root Functions
- Asynchronous Page Out
- Logical String Assist
- Integrated Coupling Migration Facility Dispatching Assist*
- Hipersorting

Availability features

- Central Processor Restart*
- System Assist Processor Reassignment*
- Subspace Group Facility
- Subsystem Storage Protection
- Concurrent Channel Maintenance
- Concurrent Power and n+1 Power
- Concurrent LIC Maintenance*
- Suppression On Protection
- Spare Memory
- Cancel I/O Request Facility
- Console Integration
- Remote Operation Support
- Local Uninterruptible Power Supply (IBM 9910)*
- Dual Utility Power Feeds*

* R2/R3 models only

S/390 Parallel Enterprise Server 9672 R1, R2, and R3 Models at a glance

Hardware	IBM S/390 Architecture			
Models and number of processors	9672-R11: 1	9672-R61: 6	9672-R42: 4	9672-R73: 7
	9672-R21: 2	9672-RA2: 1	9672-R52: 5	9672-R83: 8
	9672-R31: 3	9672-R12: 1	9672-R72: 7	9672-RX3: 10
	9672 R41: 4	9672-R22: 2	9672-R53: 5	
	9672-R51: 5	9672-R32: 3	9672-R63: 6	

Installation time	2-14 hours, new*	
	2-8 hours field upgrade (e.g. R61 to R53)*	
Channels	Minimum	3/4/3 (Parallel/ESCON/Total)
	Maximum R1	48/48/48 (Parallel/ESCON/Total)
	Maximum R2	96/128/128 (Parallel/ESCON/Total)
	Maximum R3	96/192/192 (Parallel/ESCON/Total)
	Increments	3/4 (Parallel/ESCON)*
	General	Parallel and ESCON channels are available. Configurations with OSA 1, OSA 2, or coupling links decrease channel maximums.* Model RA2 maximum 64 channels, Model R53 maximum 128 channels. R1 models have a minimum 3 ESCON channels.
Processor storage	Minimum	128MB/256MB/512MB (Model R1/R2/R3)
	Maximum	2048MB/2048MB/4096MB (Model R1/R2/R3)
	Options	128MB (Models R1, RA only), 256MB (Models R1, R2 only), 512MB, 1,024MB and 2,048MB (Model R3 only)
	General	Central and expanded storage are user-definable, Model RA2 minimum 128MB, maximum 1024MB. R1 Models minimum 128MB.
Upgradeability	Upgradeable throughout the 9672 R Model family	
	Upgradeable from 9672 R1, E, and P Models to 9672 R2 and R3 models	

Physical configuration	1 Frame	Minimum*	Weight (unpacked): 422kg (930lbs)
			Footprint: 1.0m² (10.4ft²)
			Service clearance: 2.5m² (27.4ft²)
			Input power: 0.6kVA
			Heat output: 0.6kw (2.1 kBTU/hr)
	2 Frame	Maximum*	Weight (unpacked): 1038kg (2,285lbs)
			Footprint: 1.8m² (19.7ft²)
			Service clearance: 4.8m² (51.9ft²)
			Input power: 4.2kVA
			Heat output: 4.2kw (14.3 kBTU/hr)
	General	Conforms to EIA guidelines for frames Up to three frames can be used Employs standard 24-inch cage enclosures	

Software	MVS	MVS/ESA V5R2.2, V5R2.0, V5R1.0 MVS/ESA V4R3.0, MVS/ESA V4R2.0 MVS/ESA V3R1.3 MVS/XA V2R2.0 (while supported)
	VM	VM/ESA V2R1.0 VM/ESA V1R2.2, V1R2.1, V1R1.5-370, 370 Feature (LPAR mode)
	VSE	VSE/ESA V2R1.0 VSE/ESA V1R2, 3 and 4 on RA2 and R12 in Basic model VSE/ESA V1R2, 3 and 4 on R22-RX3 in LPAR mode or as guest under VM/ESA
	TPF	TPF (Transaction Processing Facility) V4R1, TPF V3R1

* R2/3 models only

Find out more

For more information about the IBM S/390 Parallel Enterprise Server family of processors, contact an IBM marketing representative or call IBM Direct at 1 800 IBM-CALL in the United States or 1 800 IBM-4YOU in Canada, or IBM FAX at 1 800 IBM-4FAX or 1 415 855-4444. Other toll-free numbers are:

Austria	0660.5109
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Italy	167-018001
Mexico	91-800-00316
Netherlands	06-0343
Spain	900-100400
Switzerland	155 12 25

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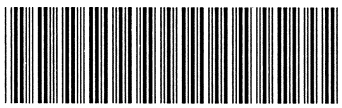

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